

BG5CT_STB_RDK Main Board Schematics

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Overview

This is the Set Top Box(STB)
Reference Design Main Board Schematic
for Marvell 88DE3288(BG5-CT) High
Definition Media Processor System on Chip

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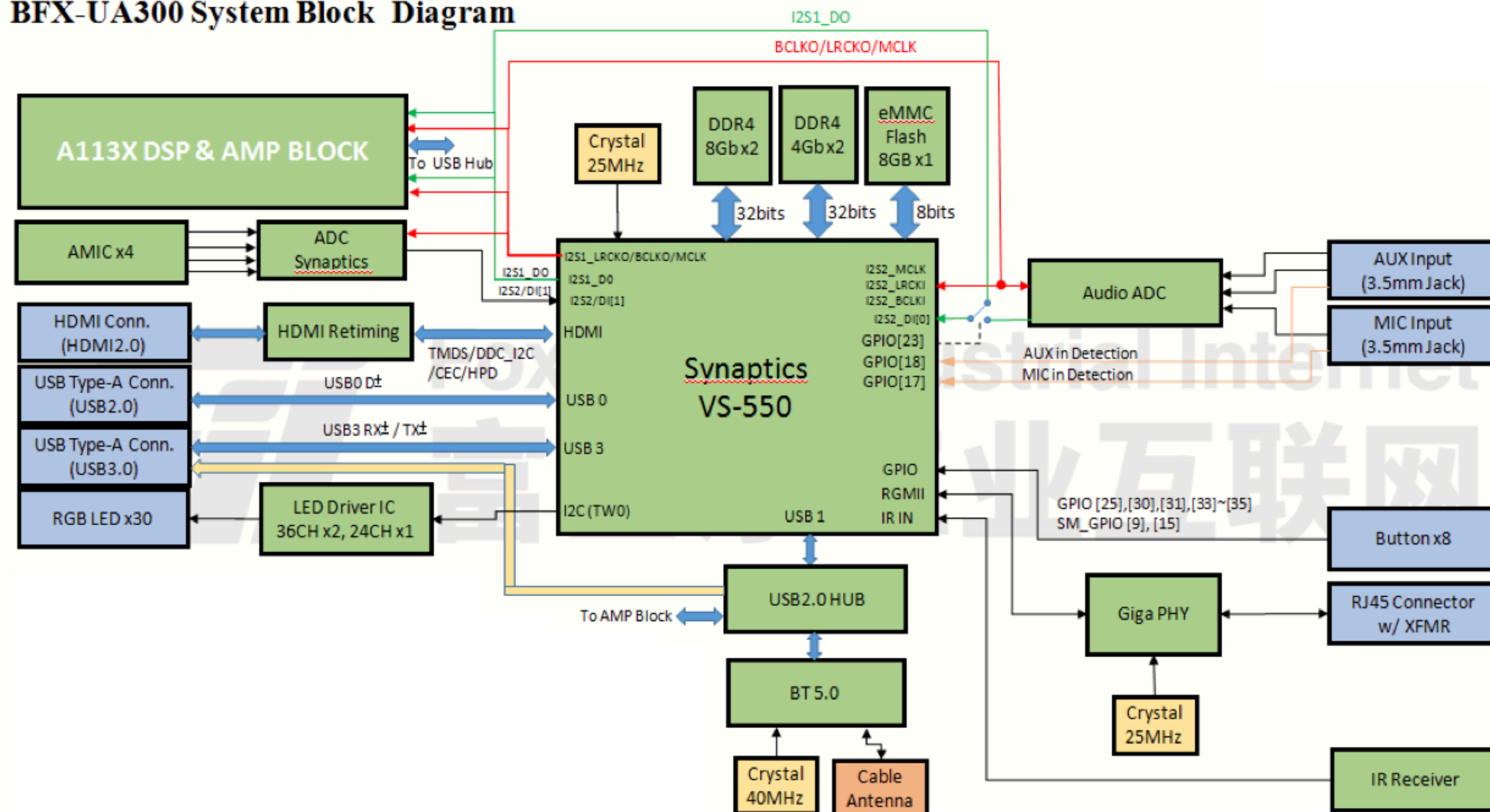
28: BT RTL8761BT

29: Power Vcpu Vgpu

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BFX-UA300 System Block Diagram

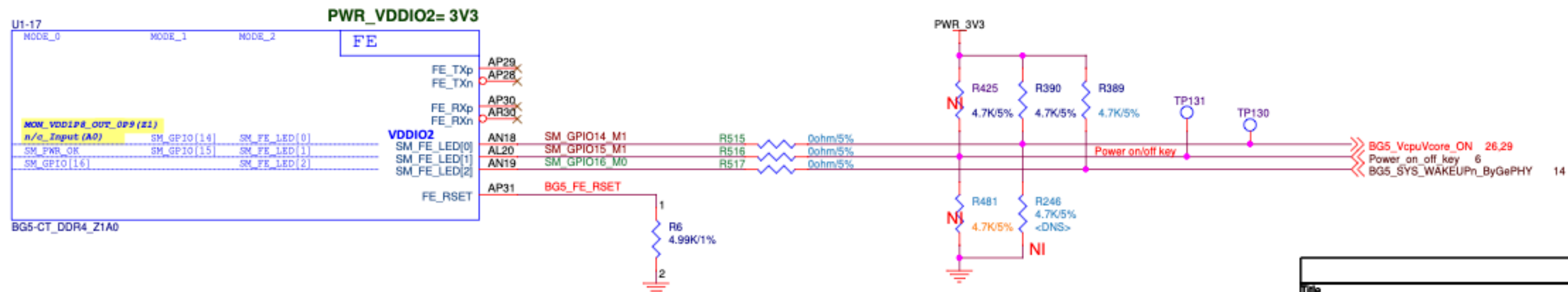
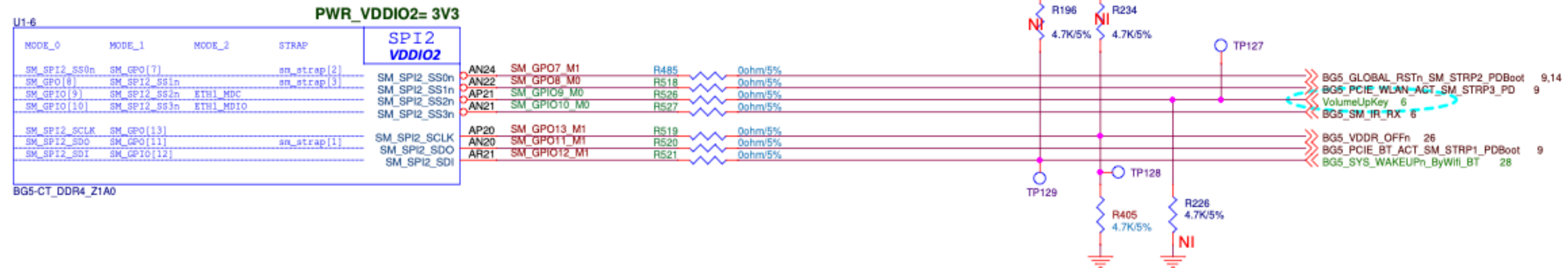
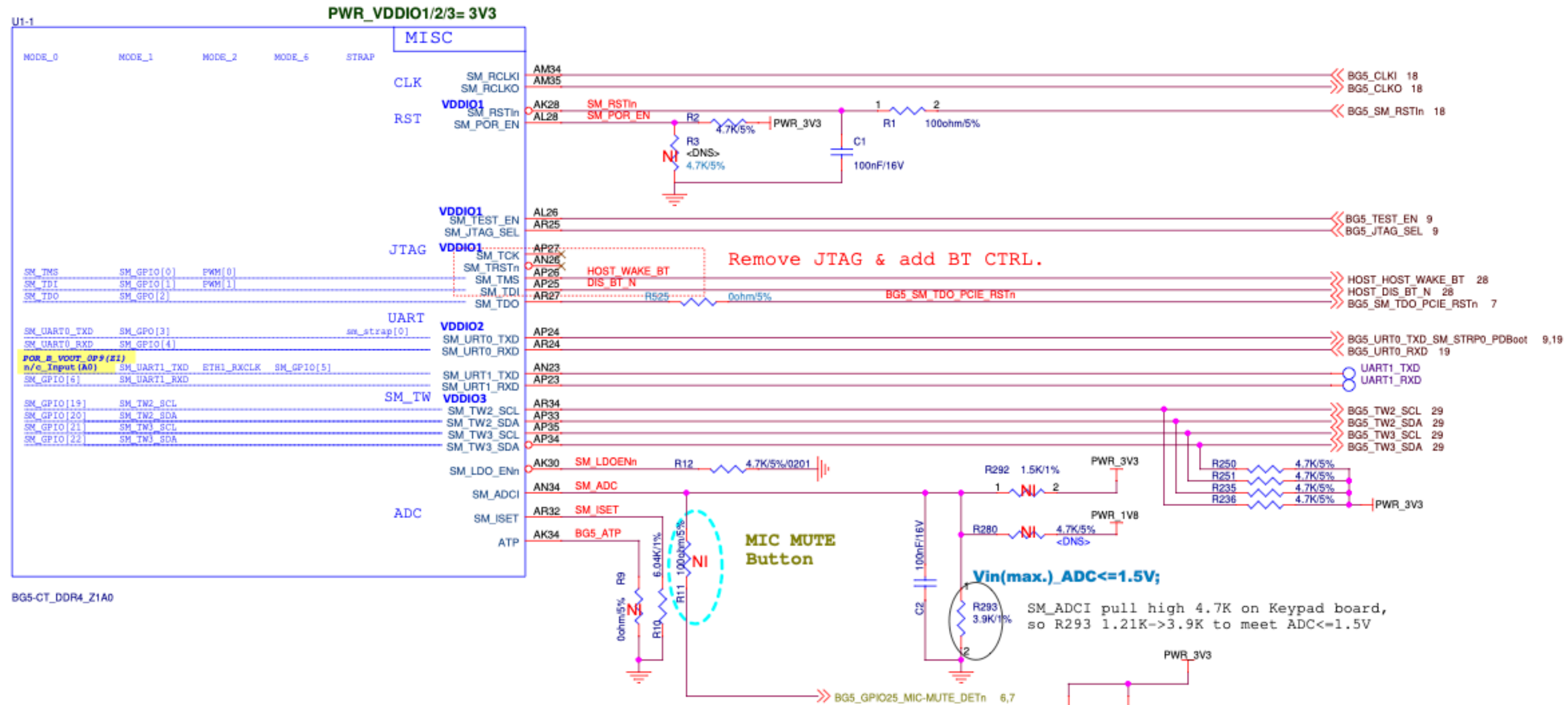


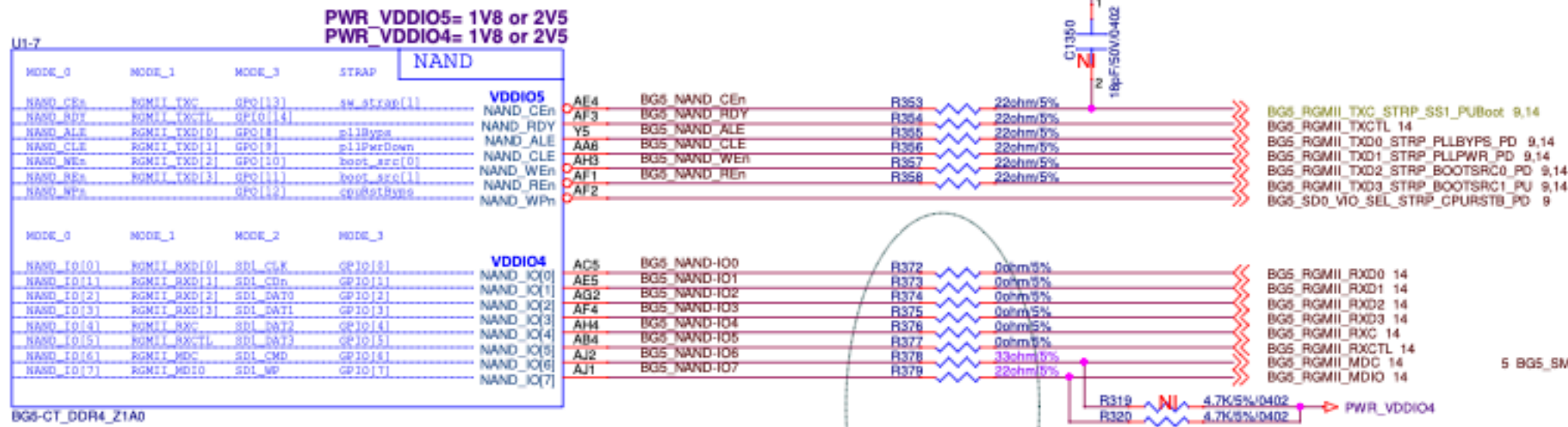
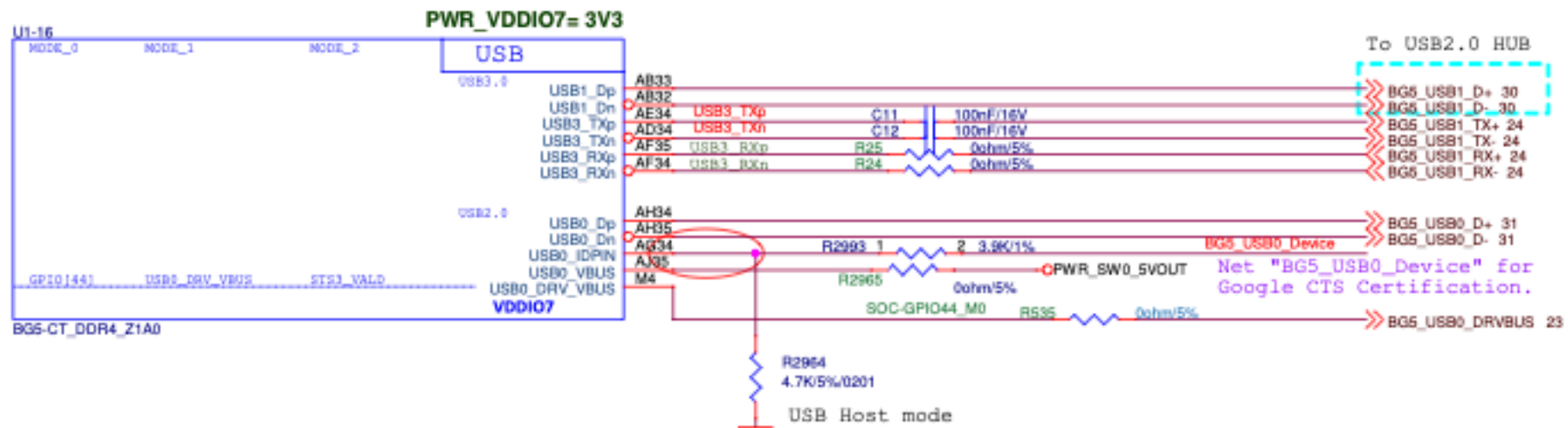
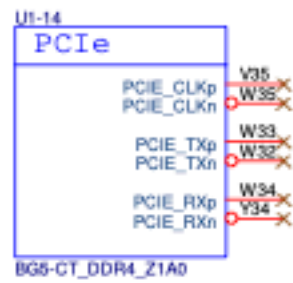
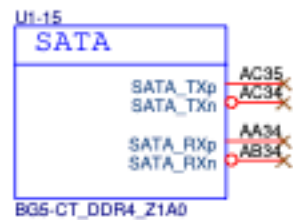
REVISION HISTORY

Version	Description
EVT1 00S0 (V005)	8-layer PCB, DDR4 8Gb x2, DDR4 4Gb x2, BT 5.0, HDMI out, USB3 x1, USB2 x1, ETN 10/100/1000, IR Receiver, Button key x8, AUX/MIC Input, RGB LED x30, AMIC x4, Audio Class-D AMP x2
EVT2 01S1 (V105)	Independent Audio Class-D circuit as a sub-board (96.1531T00)
DVT1 02S2 (V115)	1. page 5: NI R11, MIC mute button controlled by GPIO[25] 2. page 5: NI UART1, change UART BT solution to USB BT solution 3. page 5: SM_GPIO[9] to volumeUpKey 4. page 6: GPIO[32] for power down control of Class-D amplifier AD82584F 5. page 6: GPO[16] for reset control of USB2.0 HUB 6. page 6: GPIO[19] for power down control of Class-D amplifier AD83586B 7. page 6: GPIO[20] for reset control of ADC3100 8. page 6: add pull-high resistor at each button key 9. page 6: SOC USB1_Dp/Dn to upstream port of USB2.0 HUB. 10. page 7: option capacitor C1402~C1404 / C1412 / C1414~C1417 for EMI test 11. page 7: add pull-down resistor R3014 for MIC board reset control (CX20810). 12. page 7: Change MIC board CONN. from 10p/1mm WTB CONN. to 15p/0.5mm FFC CONN. 13. page 14: Changes RJ45 CONN. from tap up to tap down type. 14. page 16: Changes J814 pin4 from SPK mute to power down control of class-D AMP AD83586B. 15. page 20: add HDMI Retiming IC- IT66318. 16. page 24: Connect EM6 pin 1/2 USB2.0 HUB down stream port1. 17. page 25: change F1 from 5A to 7A and add NTC (R2904) to suppression inrush current. 18. page 25: U1308 (MP2491C), change pin 4/5 from VCC to GND; R2875 to 30K and R2876 to 20K for 5V accuracy. 19. page 27: change detect pin from pin1 to pin 6 of J805 / J806 (audio jack). 20. page 27: change AUX in (J806) from mono to stereo, ADC3100 IN2R support right CH; IN2L support left CH. 21. page 27: option capacitor C1405~C1407 / C1413 for EMI test. 22. page 27: delete C1364, R2934/R2933 0ohm (OPAMP circuit) 23. page 28: change UART BT solution to USB BT solution. 24. page 30: add USB2.0 HUB 25. EMC issue, change all WTB CONN. to FFC CONN. (J807,J808,J810) 26. EMI issue, change serial resistor from 0ohm to 120ohm bead at I2S bus (R2940~R2943,R2983,R2984,R2987) . (for MIC and AMP board CONN.) 27. Remove 0ohm resistor (R2980~R2982, R2986,R2991,R2992) at J814 circuit (AMP board CONN.), because AMP board GND no EMI issue and good GND contact for EMC test)
DVT2 03S3 (V115)	1. Page 14: Change Ethernet PHY RX/TX to no delay: no mount R813 / R815, mount R812 / R814. 2. Page 20: Change RX side capacitors of HDMI retiming IC from 0.1uF to 0ohm (C15,C16,C17,C19,C20,C1427,C1428,C1429)
DVT3 04S4 (V125)	1. Page 6: Change GPIO[32] net define as "CTRL_A113X" and GPIO[19] as "AMP_PWM_OFF". 2. Page 6: R138, R139 4.7Kohm -> 820ohm, improve I2C CLK/DAT rising time 3. Page 7: Add GPIO[24] as IO24_USB_SW_S for USB switch control and GPIO[27] as "IO27_AMP_Reset" for AMP IC reset. 4. Page 7: Add buffer IC (U1321) at I2S bus. 5. Page 16: Add buffer IC (U1320) at I2S bus and change pin define of pin 1/2/4/6 of J814. 6. Page 23: USB2.0 CONN. D-/D+ connect to USB SW circuit. 7. Page 24: NI R2857, mount R2852, pull EN pin of USB3.0 port power SW to inhance USB3.0 port hot-plug detect. 8. Page 27: Add buffer IC (U1319) at I2S bus. 9. Page 30: Add nets at pin DM3/DP3 of USB HUB for A113X software download. 10. Page 30: NI R3009, enable port 3 of USB HUB, for A113X SW download patch. 11. Page 31: Option USB SW circuit for A113X software download.
Pre-MP 05S5 (V135)	1. Page 07: C1414: NI->39pF, C1415/C1417: NI->27pF, follow ALT EMI debugging points 2. Page 07: R308: Res. 33ohm -> FB 120ohm, C1403: NI->20pF, follow ALT EMI debugging points 3. Page 16: Add one N-MOSFET at EN pin of U1320 and add two N-MOSFET at I2C bus. To disconnect I2C/I2S bus with SOC during passive standby mode, ensure power sequence is correct of A113X after wakeup. 4. Page 16: No mount R2987 and R3064, because AMP board (A113X) no MCLK requirement. 5. Page 16: C1408/C1409/C1411: NI->27pF, follow ALT EMI debugging point 6. Page 27: C1406/C1407: NI->27pF, follow ALT EMI debugging point

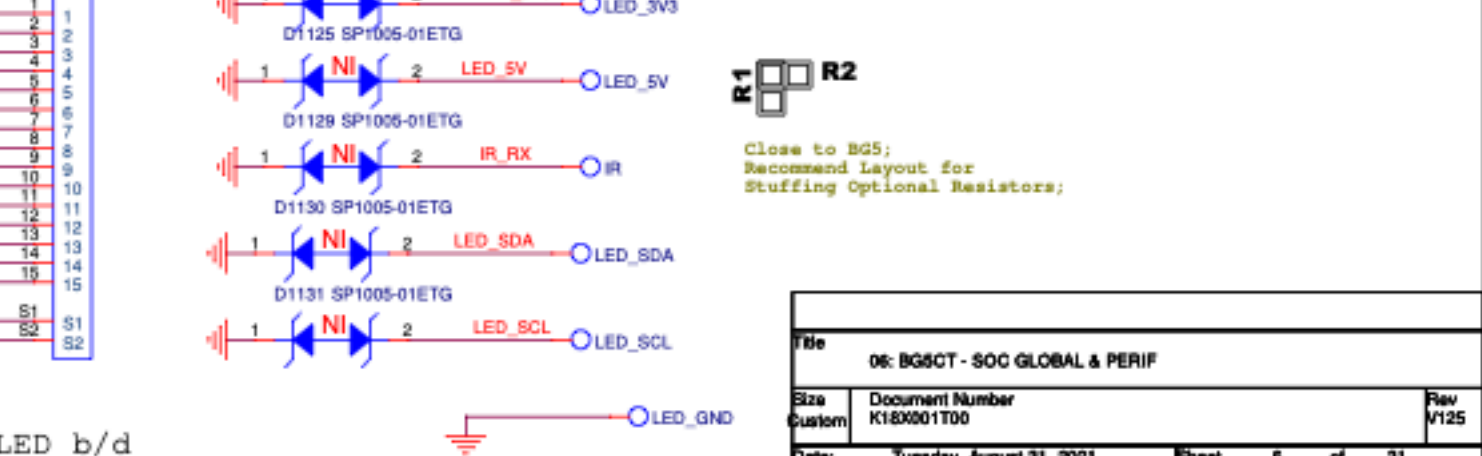
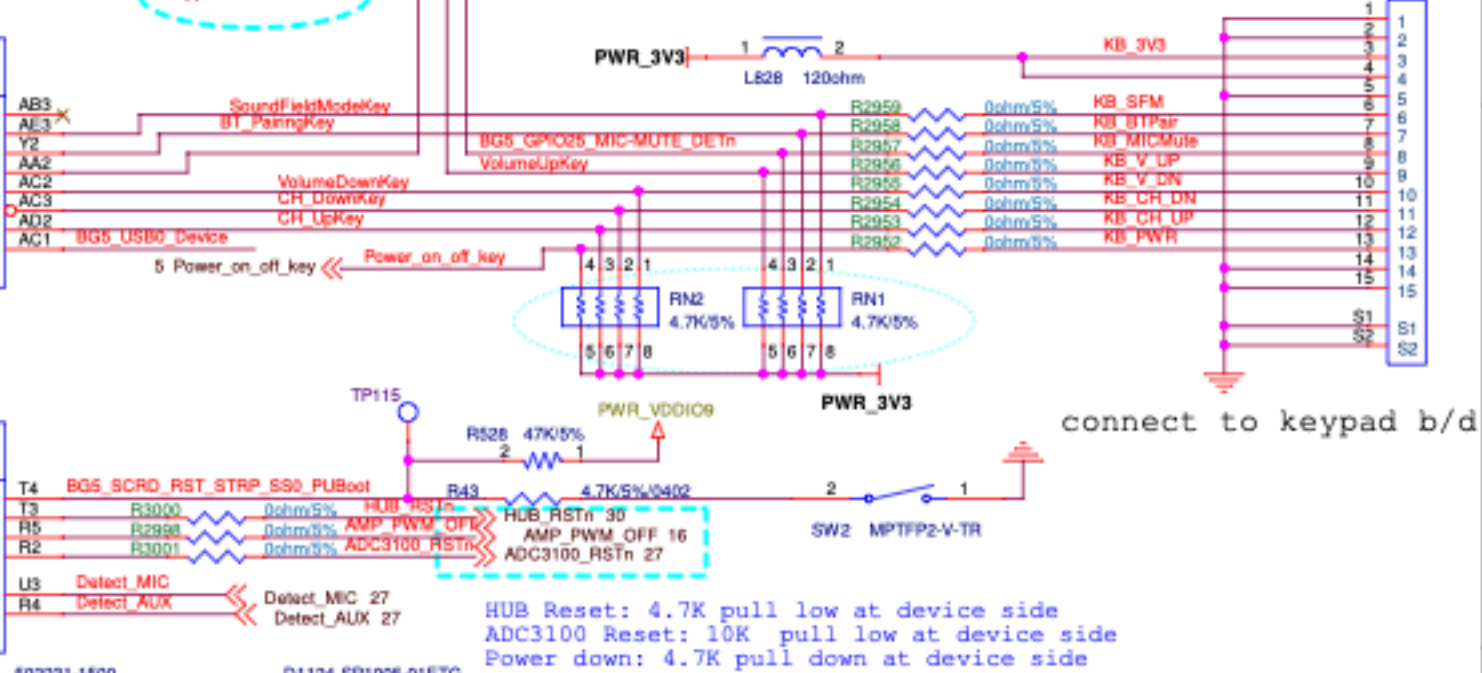
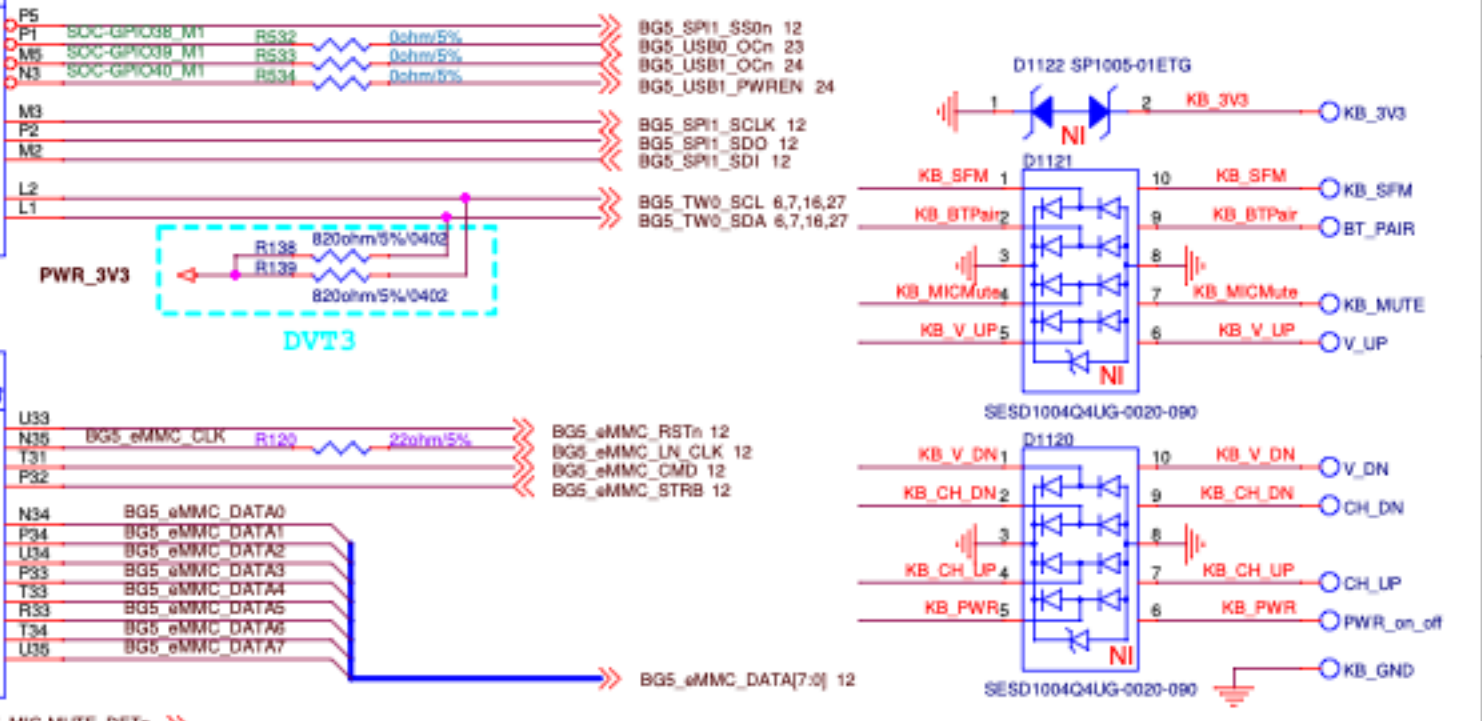
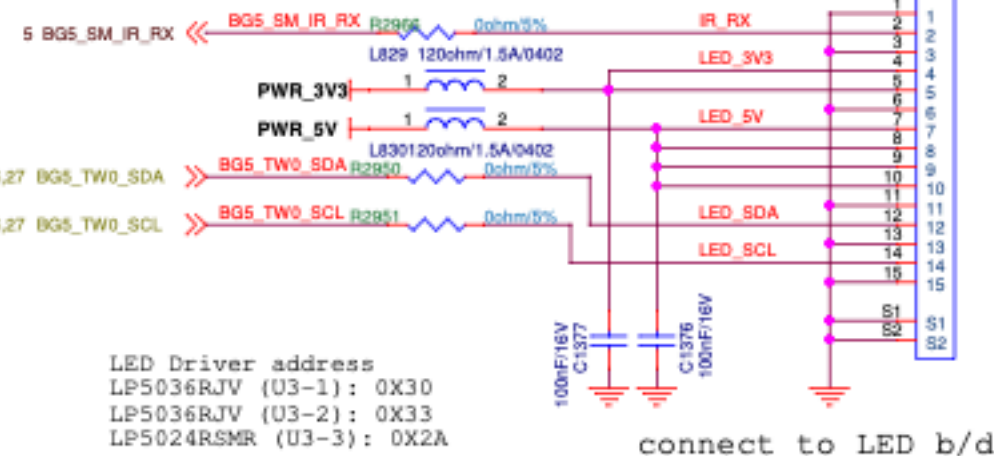
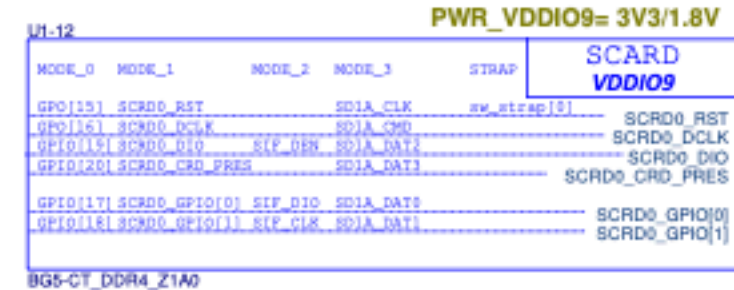
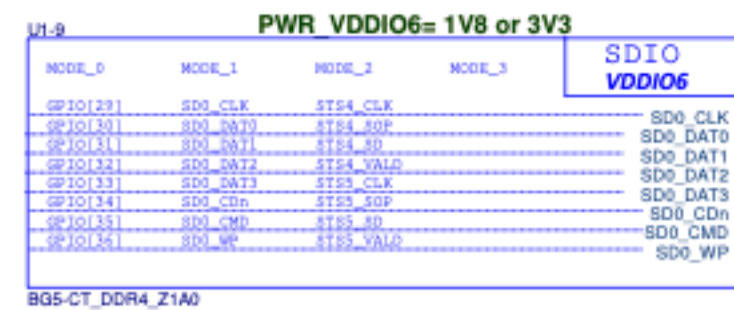
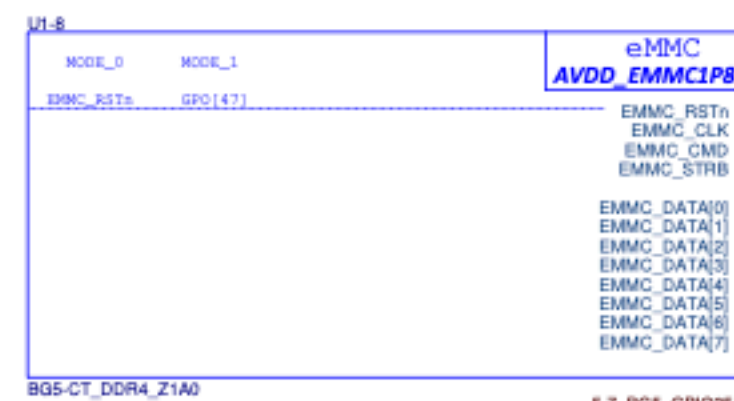
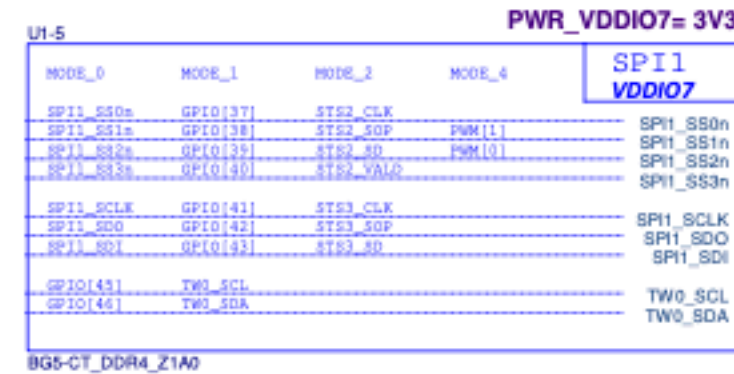
Revision History		
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Date:	Tuesday, August 31, 2021	Sheet 3 of 31

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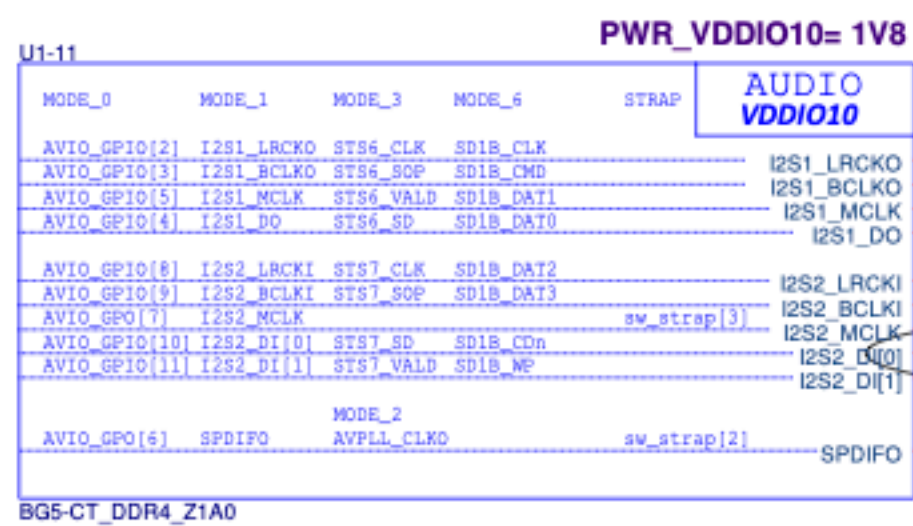
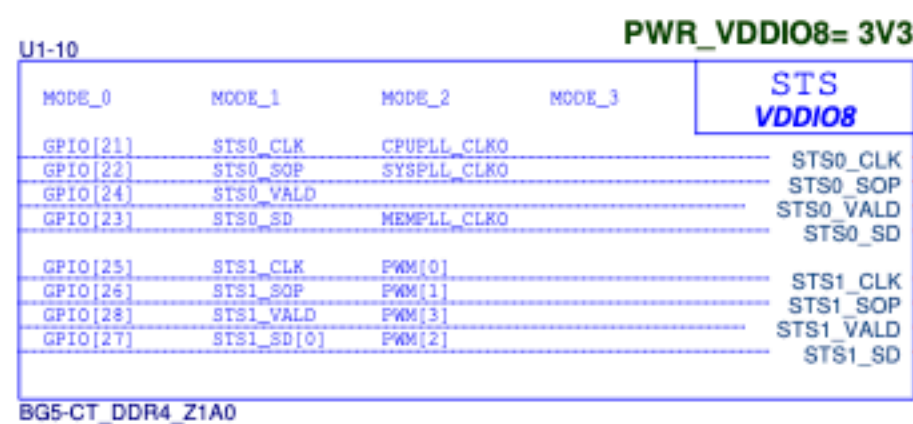
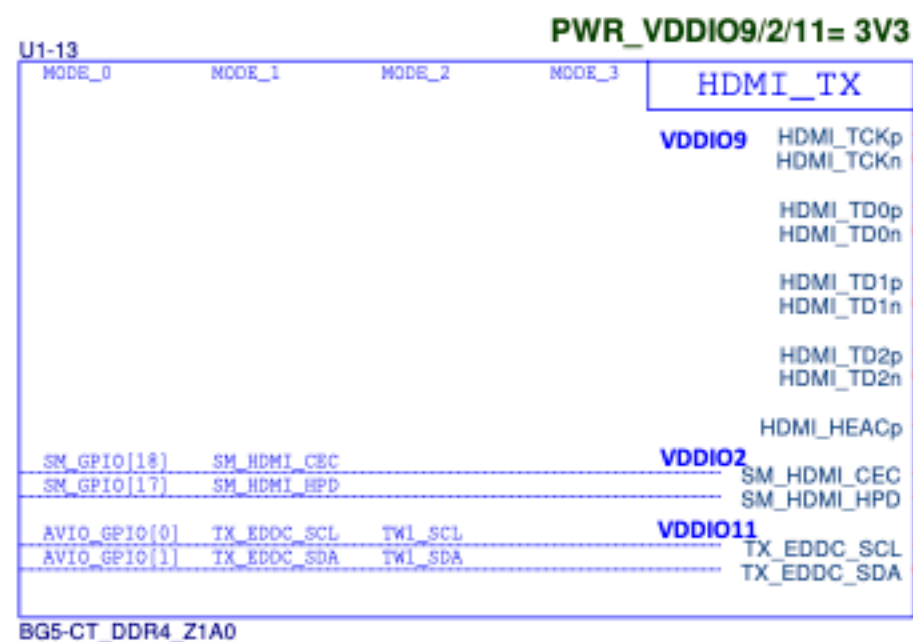




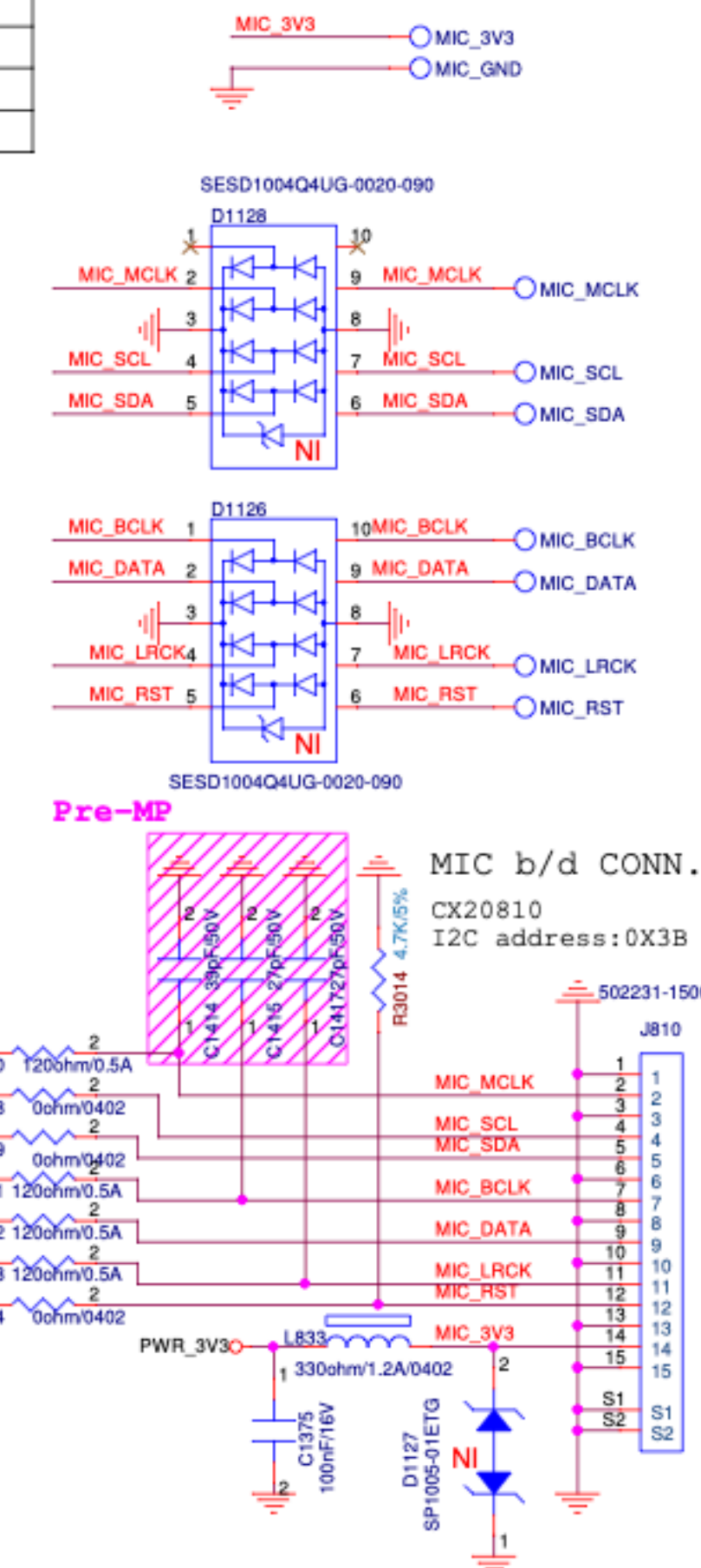
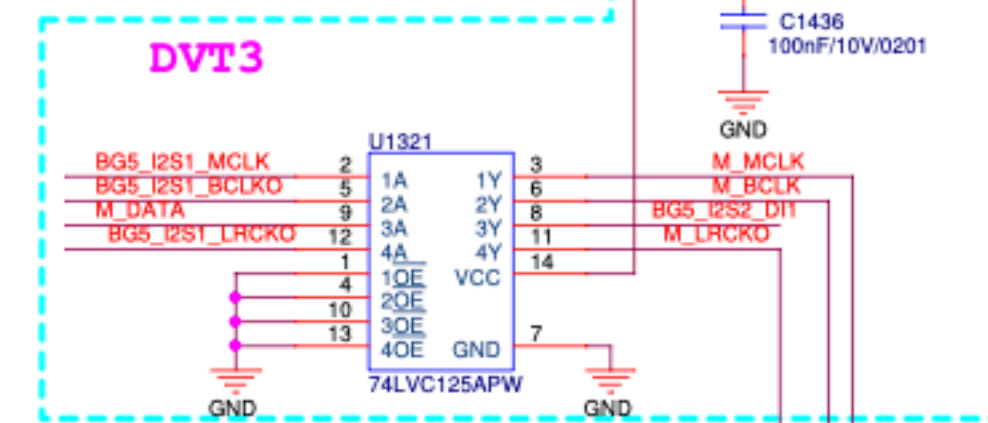
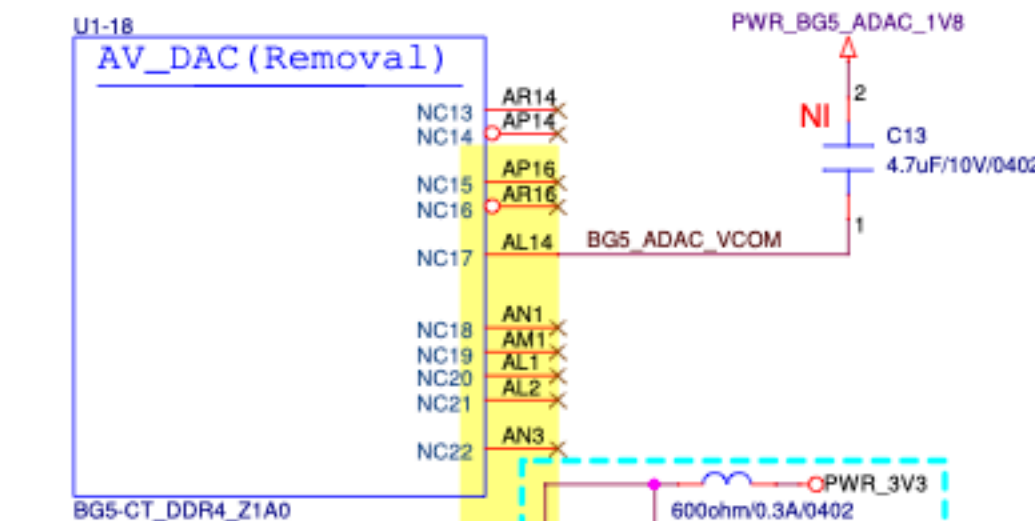
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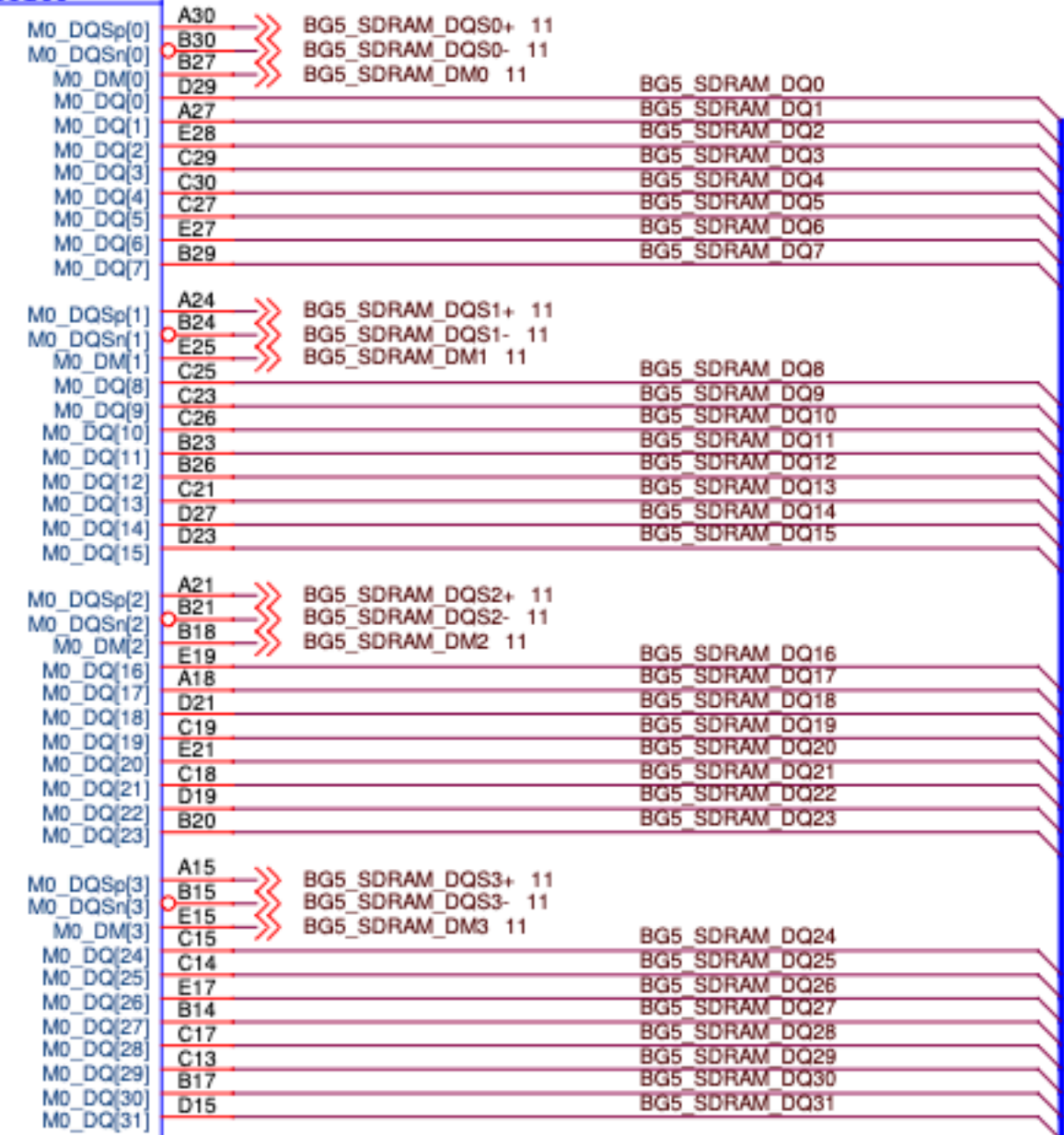
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Date	Tuesday, August 31, 2021	Sheet	6 of 31



BG4CT TMDs Configuration in STB		
Ball# in BG4CT	Ball Definition in BG4CT	Pin Definition in HDMI Connector
AP13	HDMI_TX_TCKp	HDMI_TD2-
AR13	HDMI_TX_TCKn	HDMI_TD2+
AP11	HDMI_TX_TD0p	HDMI_TD1+
AR11	HDMI_TX_TD0n	HDMI_TD1-
AP10	HDMI_TX_TD1p	HDMI_TD0+
AP9	HDMI_TX_TD1n	HDMI_TD0-
AR8	HDMI_TX_TD2p	HDMI_TCK-
AP8	HDMI_TX_TD2n	HDMI_TCK+

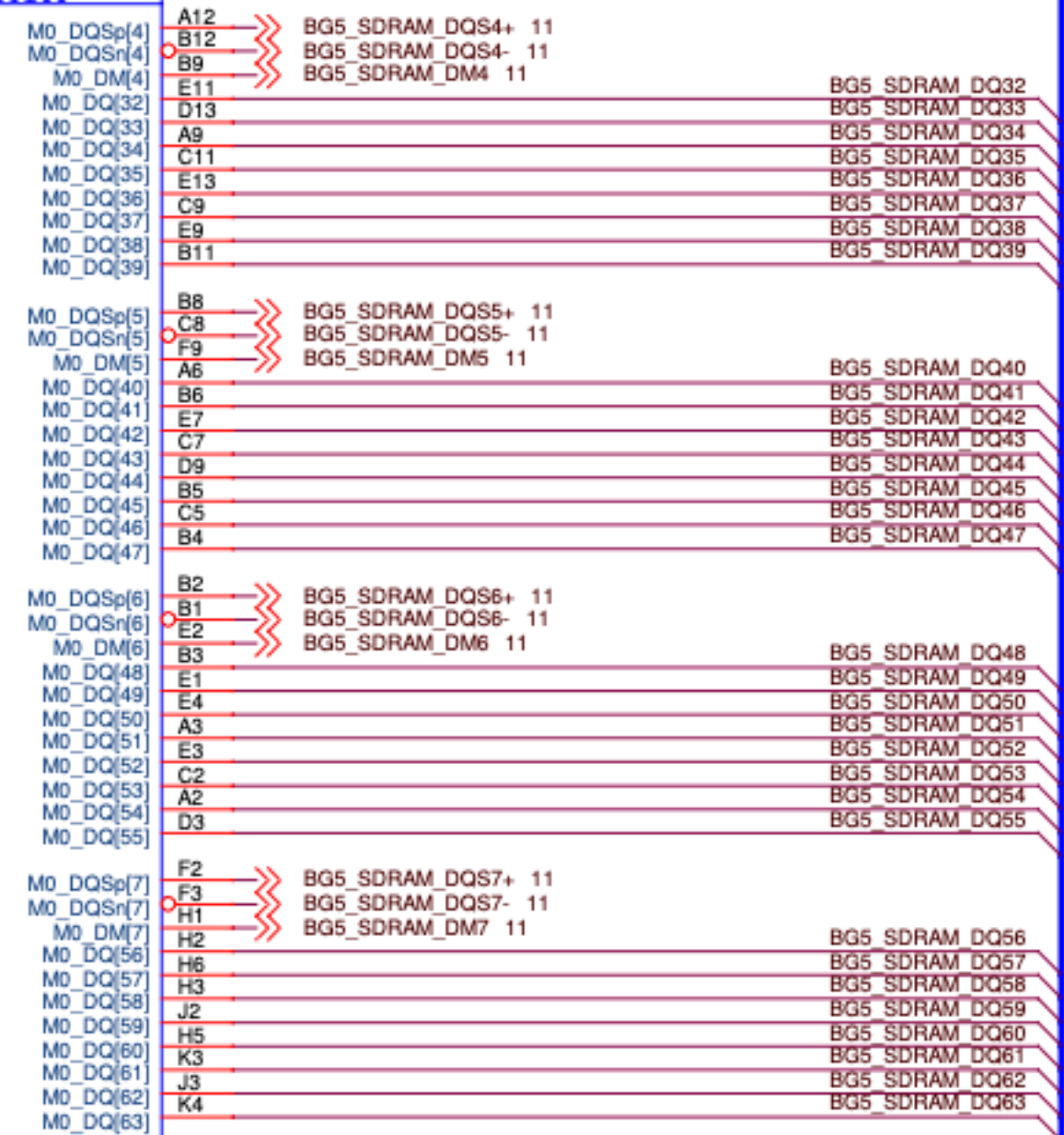


U1-3 DDR4 SDRAM - DATA



BG5-CT_DDR4_Z1A0

U1-4 DDR4 SDRAM - DATA



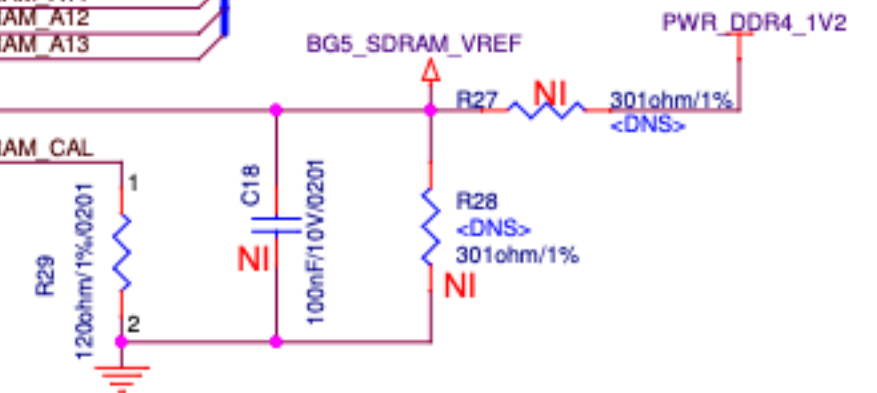
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U1-2 DDR4 SDRAM - ADD/CTL

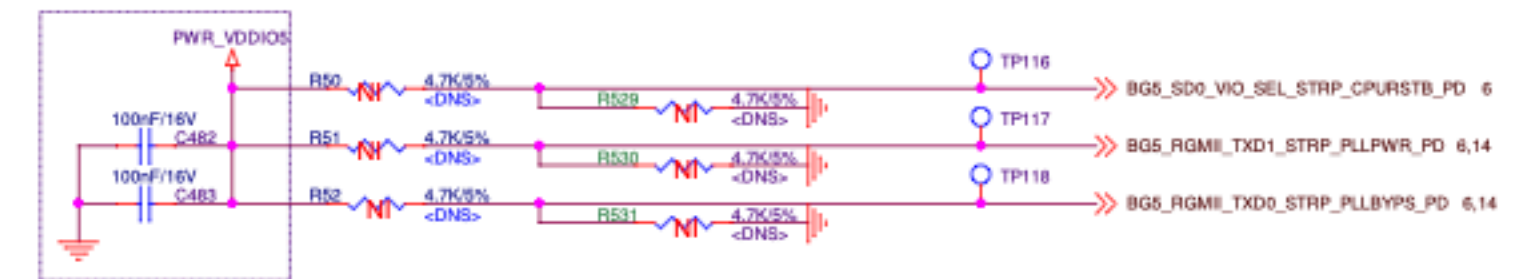
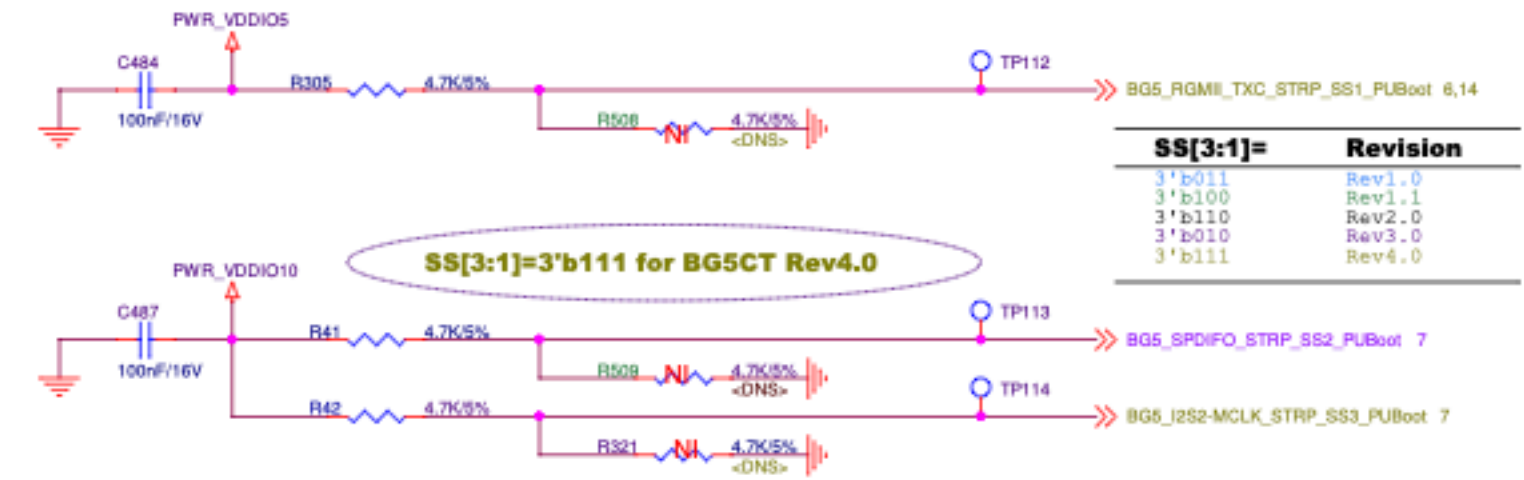


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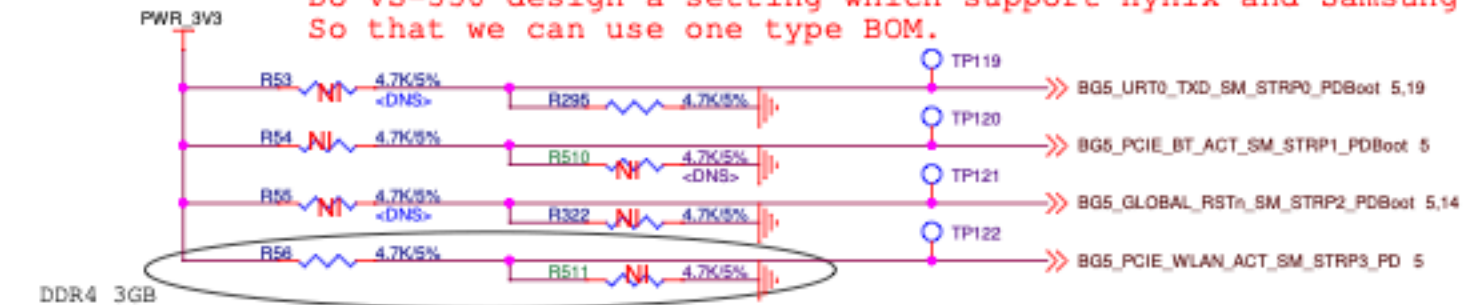


Title		
08: BG5CT - DDR4 PHY		
Size	Document Number	Rev
Custom	K18X001T00	V125
Date:	Tuesday, August 31, 2021	Sheet 8 of 31

S.No	Pad Name	Strap name in pinList	Description	Reg in global BIU	on-chip PUPD	
1	SPDIFO	software_strap[2]	Straps for software usage	FRR_Gbl_ubootStrap_softwareStrap bit 2	N/A	
2	I2S2_MCLK	software_strap[3]	Straps for software usage	FRR_Gbl_ubootStrap_softwareStrap bit 3	N/A	
	SCRD0_RST	software_strap[0](USB_BOOTn)	Straps for software usage ROM code will use this strap to decide booting from USB or not 0: Boot from USB	FRR_Gbl_ubootStrap_softwareStrap bit 0	PU	
3						
4	NAND_CEn	software_strap[1]	Straps for software usage	FRR_Gbl_ubootStrap_softwareStrap bit 1	PD	
5	NAND_REn	boot_src[1]	CPU Boot Source bit[1] 00: ROM boot from SPI 01: NAND 10: ROM boot from EMMC 11: Direct boot from SPI(Only available when ENG_EN=1) When direct boot from SPI(SPI clear boot), pwrCntlByps and cpuRstByps should be set to 1, pllByps Strap should be set to 0, pllPwrDown should be set to 0	FRR_Gbl_ubootStrap_bootSrc bit 1	N/A	
	NAND_WEn	boot_src[0]	CPU boot source bit[0] 00: ROM boot from SPI 01: NAND 10: ROM boot from EMMC 11: Direct boot from SPI(Only available when ENG_EN=1) When direct boot from SPI(SPI clear boot), pwrCntlByps and cpuRstByps should be set to 1, pllByps Strap should be set to 0, pllPwrDown should be set to 0	FRR_Gbl_ubootStrap_bootSrc bit 0	N/A	
6						
	NAND_WPn	cpuRstByps	CPU reset bypass strap 0: Enable reset logic inside cpu partition 1: Bypass reset logic inside cpu partition	FRR_Gbl_ubootStrap_cpuRstByps	PD	
7						
	NAND_CLE	pllPwrDown	SYSTEM/CPU PLL Power Down 1: Power Down 0: Power UP	FRR_Gbl_ubootStrap_pllPwrDown	PD	Power Down Pll if no pull down resistor on board
8						
	NAND_ALE	pllByps	SYSTEM/CPU PLL Bypass indicator 0: No Bypass 1: All PLL Bypassed	FRR_Gbl_ubootStrap_sysPlkByps FRR_Gbl_ubootStrap_memPlkByps FRR_Gbl_ubootStrap_cpuPlkByps	PD	
9						
	SM_URT0_TXD	SM_STRP[0]	SM to SOC RSTn mode select 0: SM_SOC_RSTn_DO_FModule releasing waits for SoCRstCnt but does not wait for SM_PWR_OK(mode_0 of SM_FE_LED[1], system will assert this signal when SOC core power is ready). 1: SM_SOC_RSTn_DO_FModule releasing waits for both SoCRstCnt and SM_PWR_OK.		PD	
10						
	SM_SPI2_SDO	SM_STRP[1]	software strap		PD	
11						
12	SM_SPI2_SS0n	SM_STRP[2]	software strap		PD	
13	SM_SPI2_SS1n	SM_STRP[3]	software strap		PD	



Original DDR4 setting is not in the "Part Stuffing Guide".
Do VS-550 design a setting which support Hynix and Samsung DDR4?
So that we can use one type BOM.

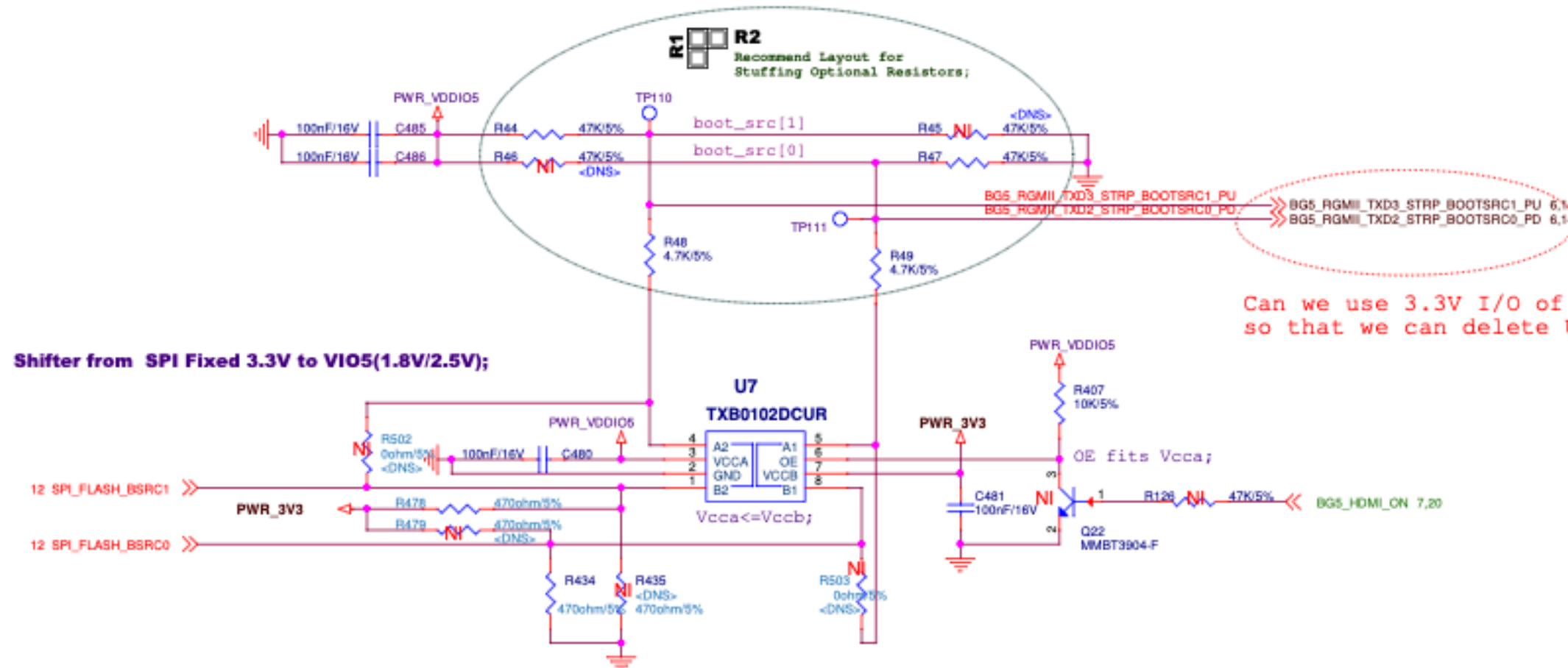


Part Stuffing Guide for DDR Vendor on SM_STRP[3:1]

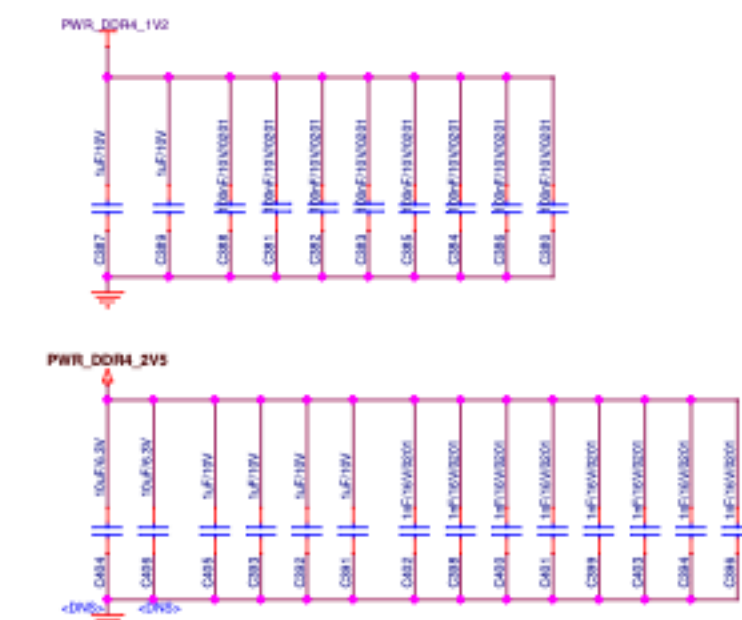
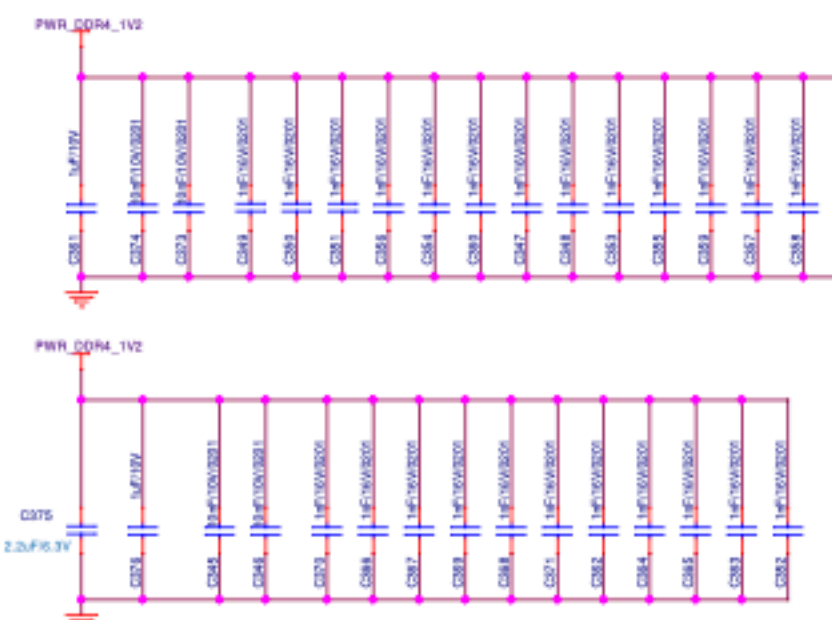
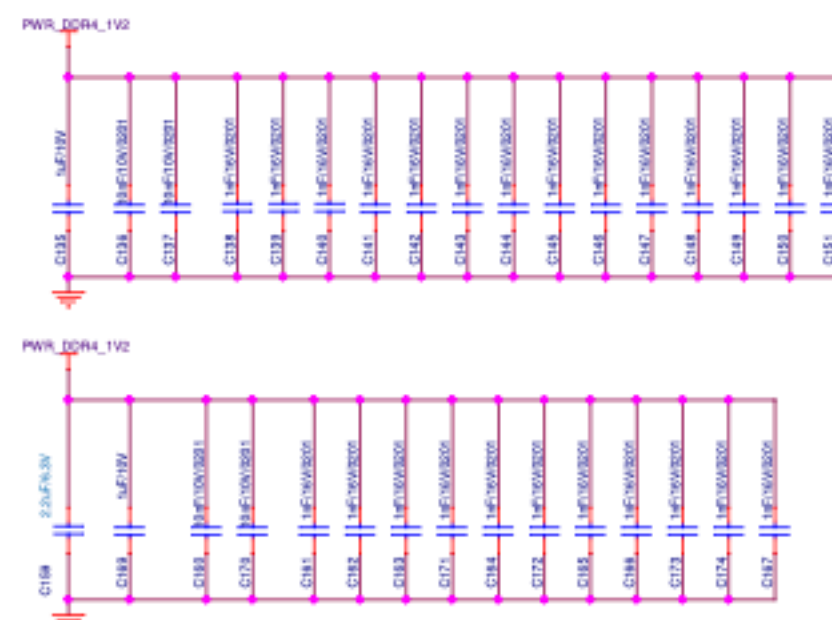
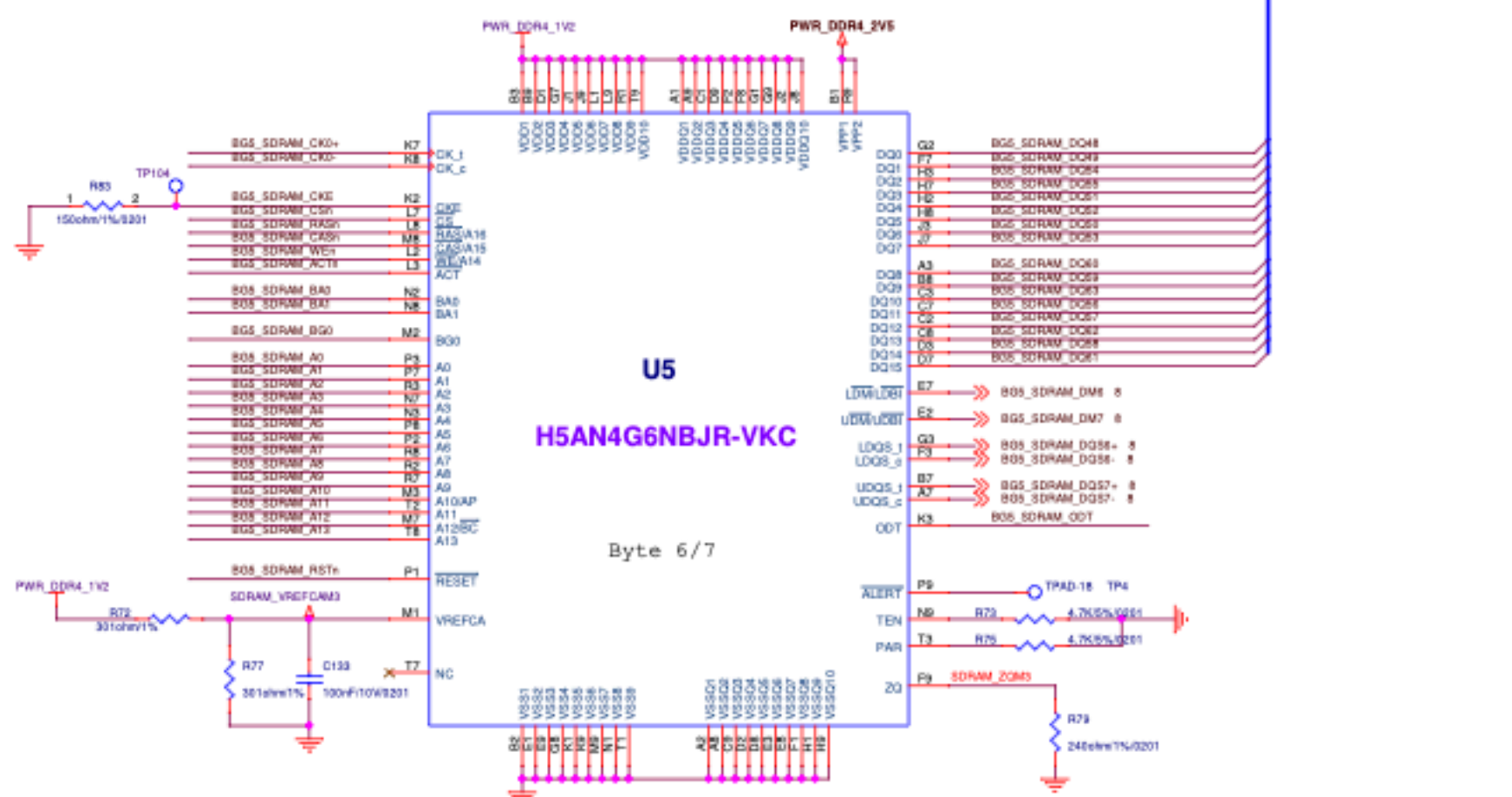
Vendor	SM_STRP [3]	SM_STRP [2]	SM_STRP [1]	Stuffed	Non-Stuffed
Hynix	0	Reserved	0	R511/R510	R54/R55/R56
Samsung	1	Reserved	0	R56/R510	R54/R55/R511
Micron	0	Reserved	1	R54/R511	R510/R55/R56
Reserved	1	Reserved	1	R54/R56	R511/R55/R510



Can we use 3.3V I/O of VS-550,
so that we can delete U7 (level shift)



File	09: BG5CT - PIN STRAP
Size	Document Number
Custom	K18X001T00
Date	Tuesday, August 31, 2021
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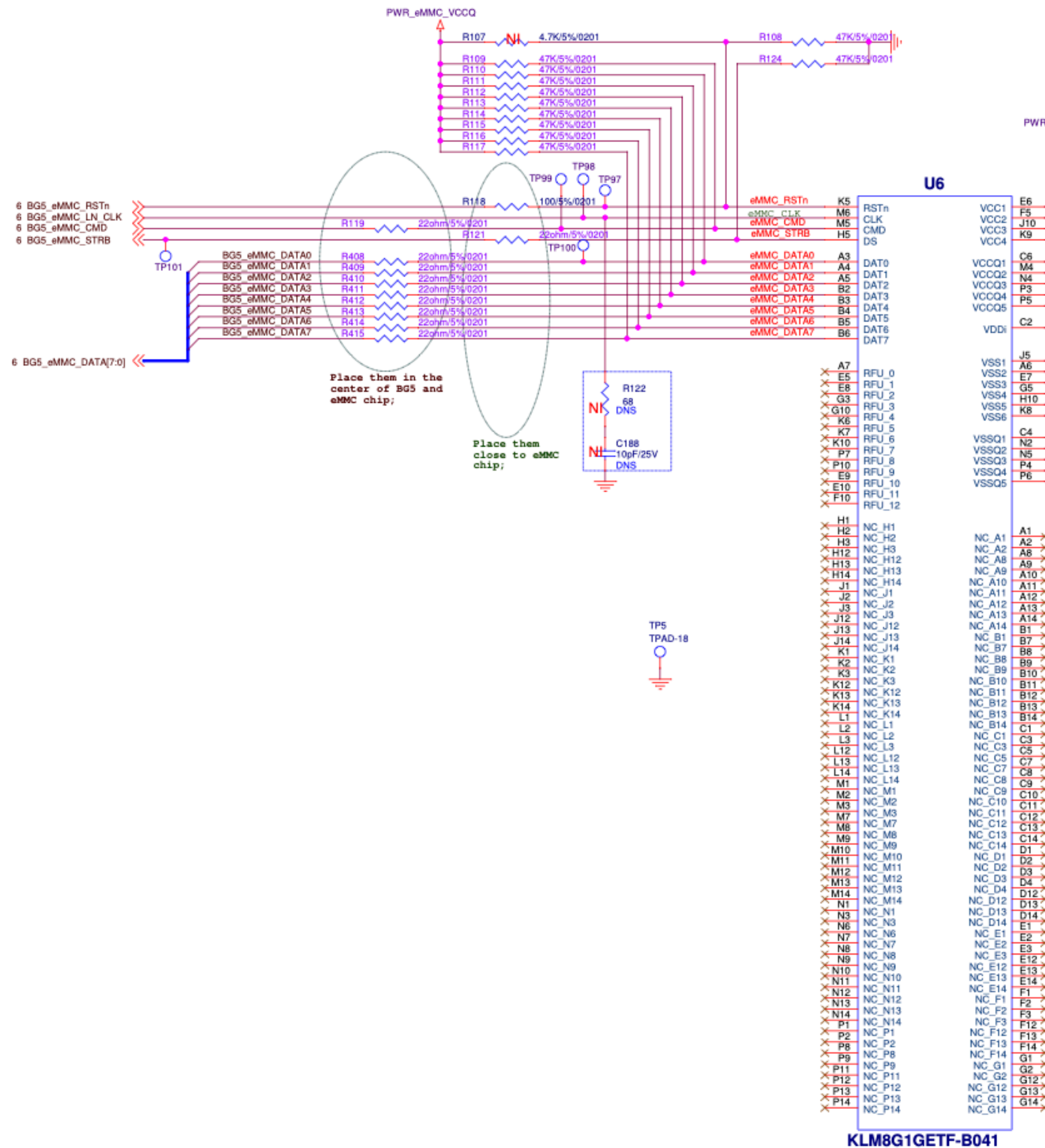
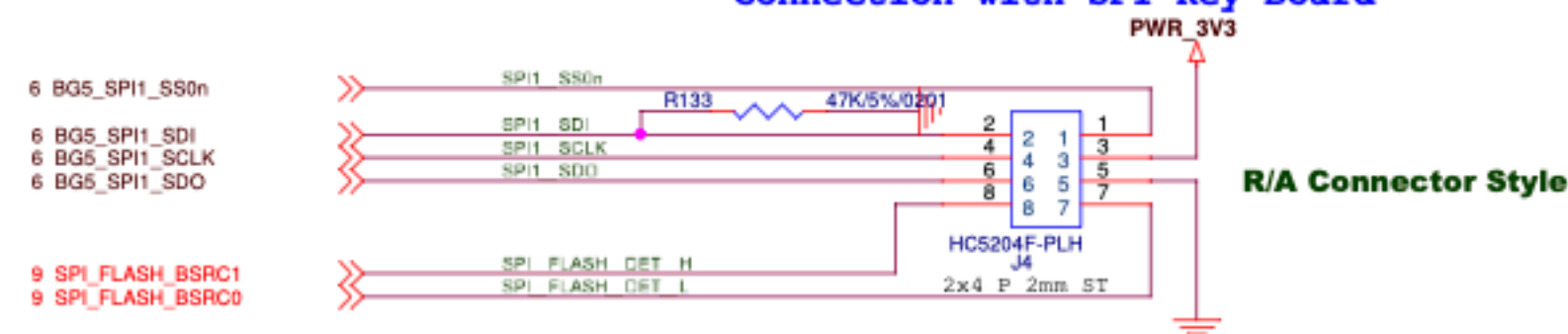


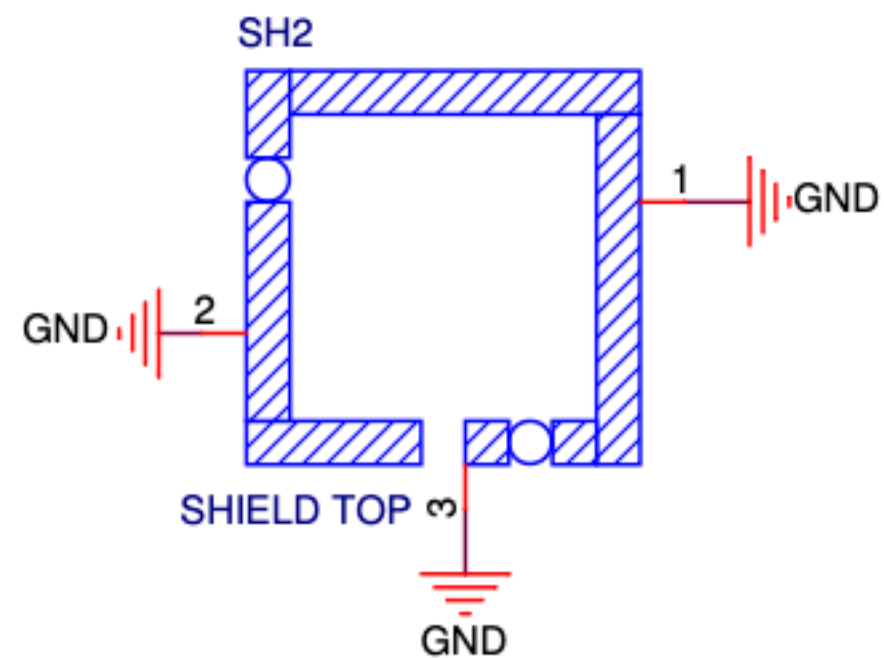
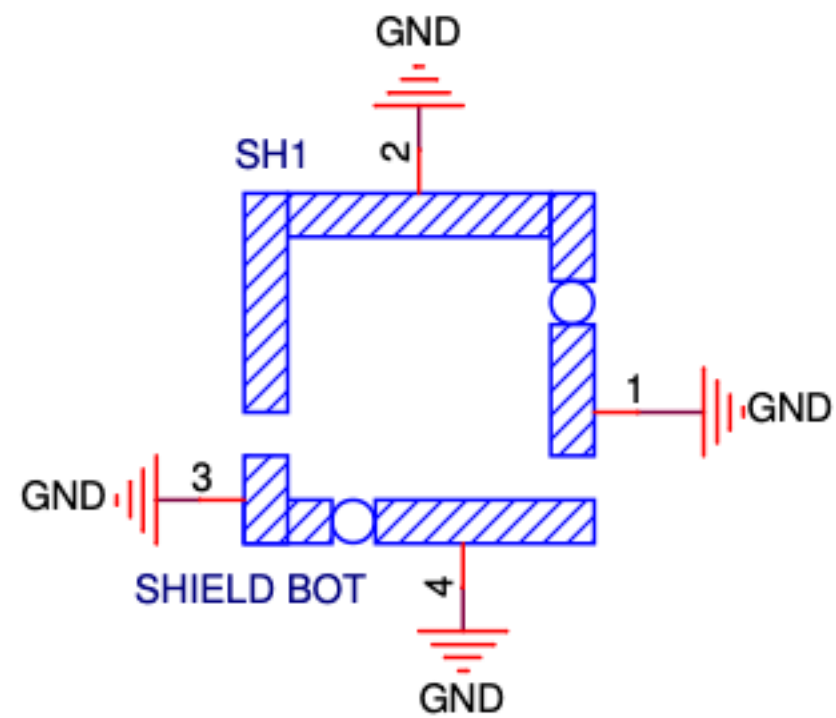
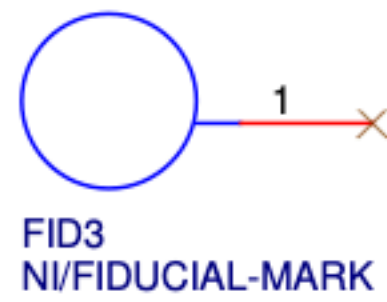
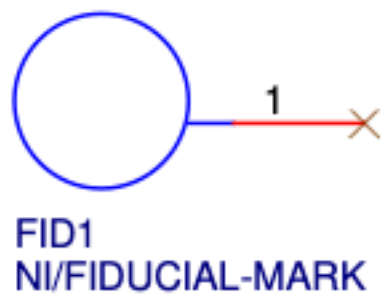
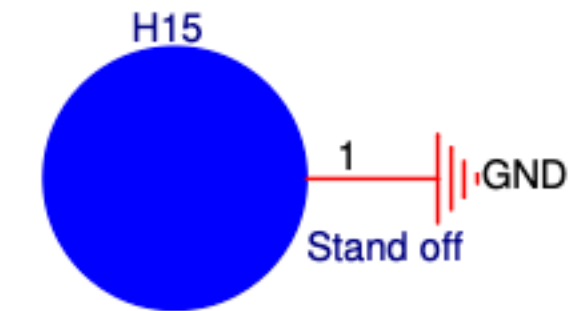
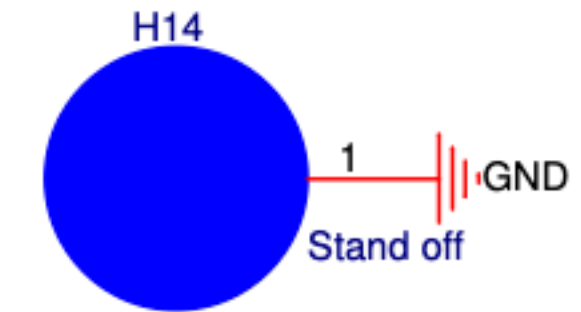
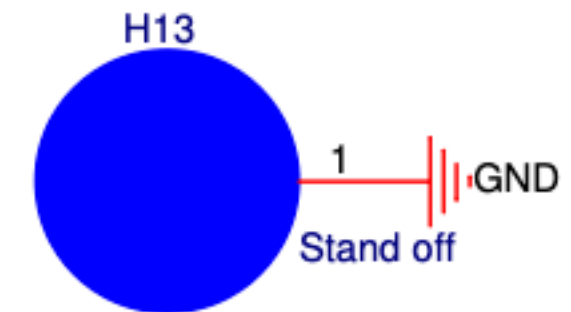
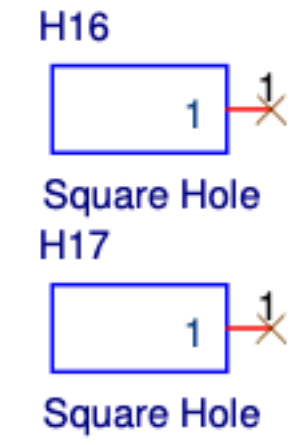
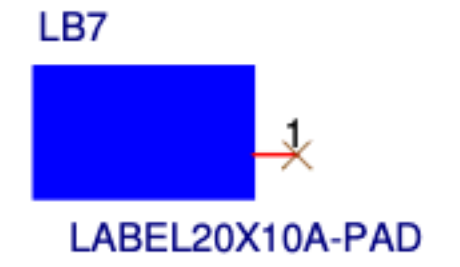
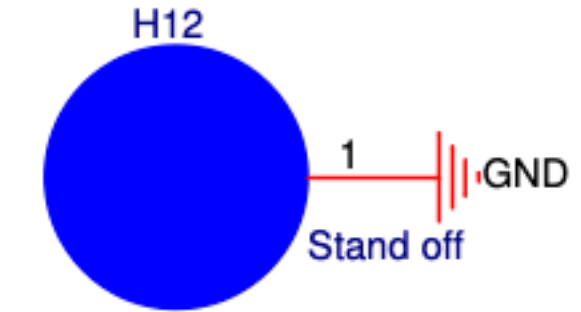
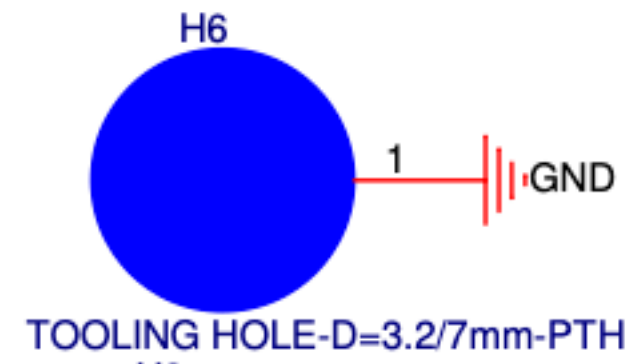
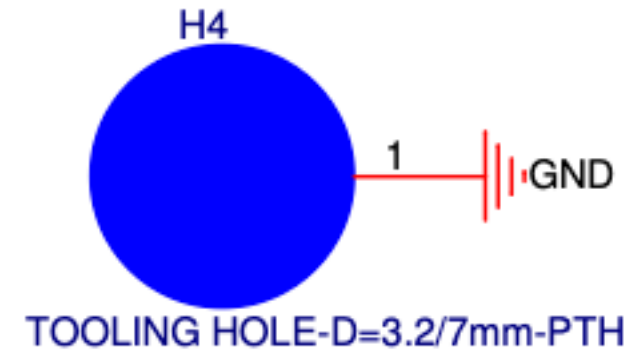
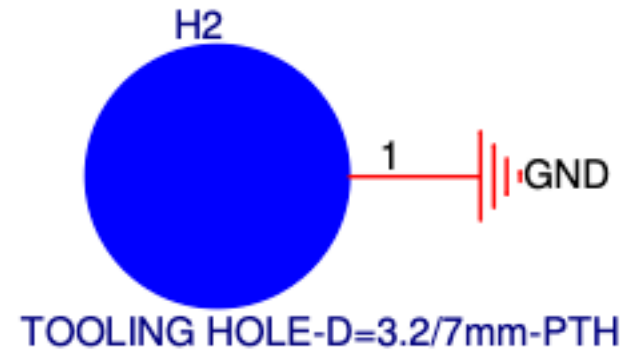
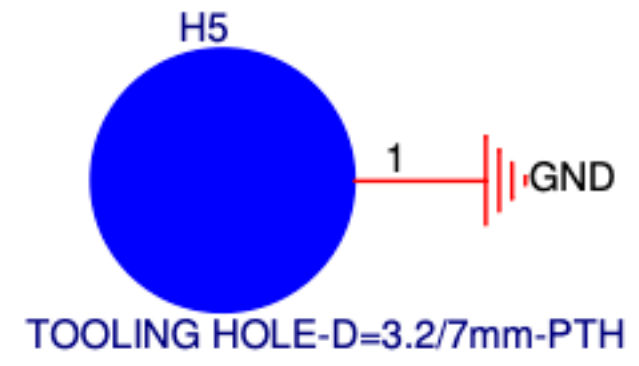
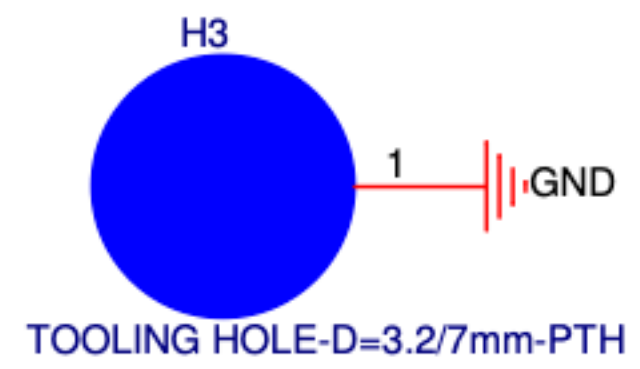
Table 178 — eMMC voltage combinations

V _{cc}	V _{ccQ}	V _{ccQ}		
		1.1V-1.3V	1.70V-1.95V	2.7V-3.6V
		Valid	Valid	Valid (1)
	2.7V-3.6V	Valid	Valid	Valid (1)
	1.7V-1.95V	Valid	Valid	NOT VALID

(1) V_{ccQ} (I/O) 3.3 volt range is not supported in either HS200 or HS400 devices

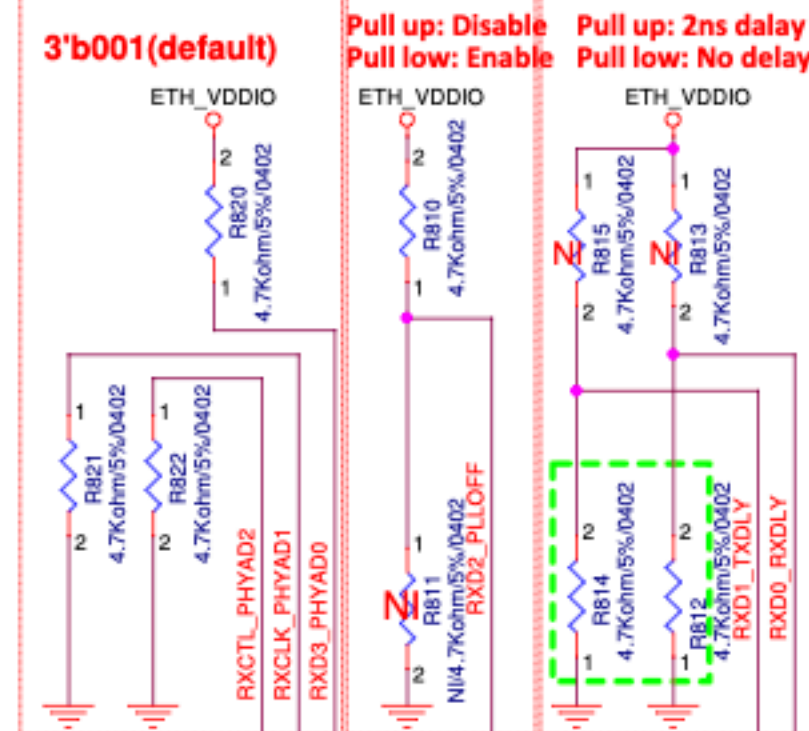
Connection with SPI Key Board





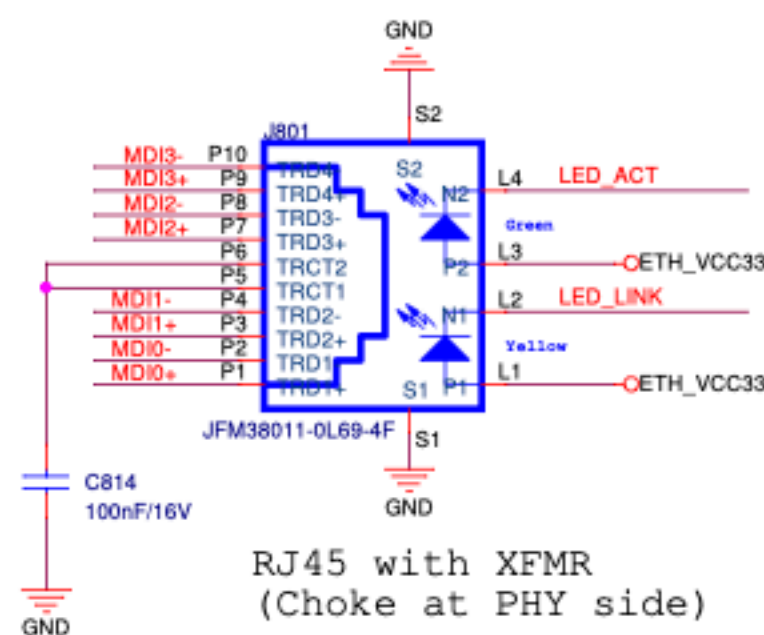
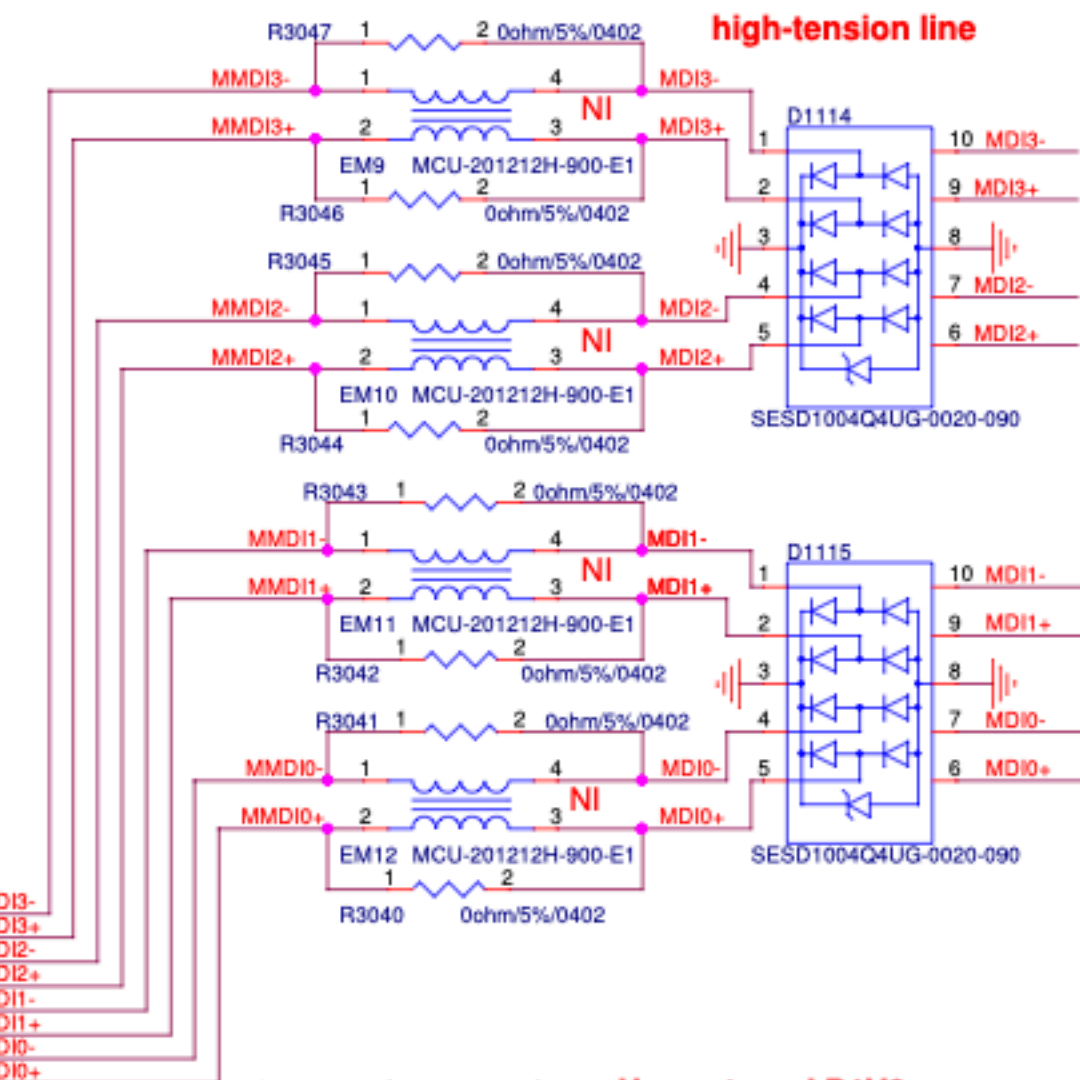
Title		
13: PERIF - NGFF Module @SD1_NA		
Size A	Document Number K18X001T00	Rev V125
Date:	Tuesday, August 31, 2021	Sheet 13 of 31

PHY Address Config. Disable/Enable PLL RGMII TXC/RXC Delay Config



SOC Vendor: TX & RX delay 2ns
GMI : TX no delay, RX delay 2ns
ALT claim FXN change to no delay.

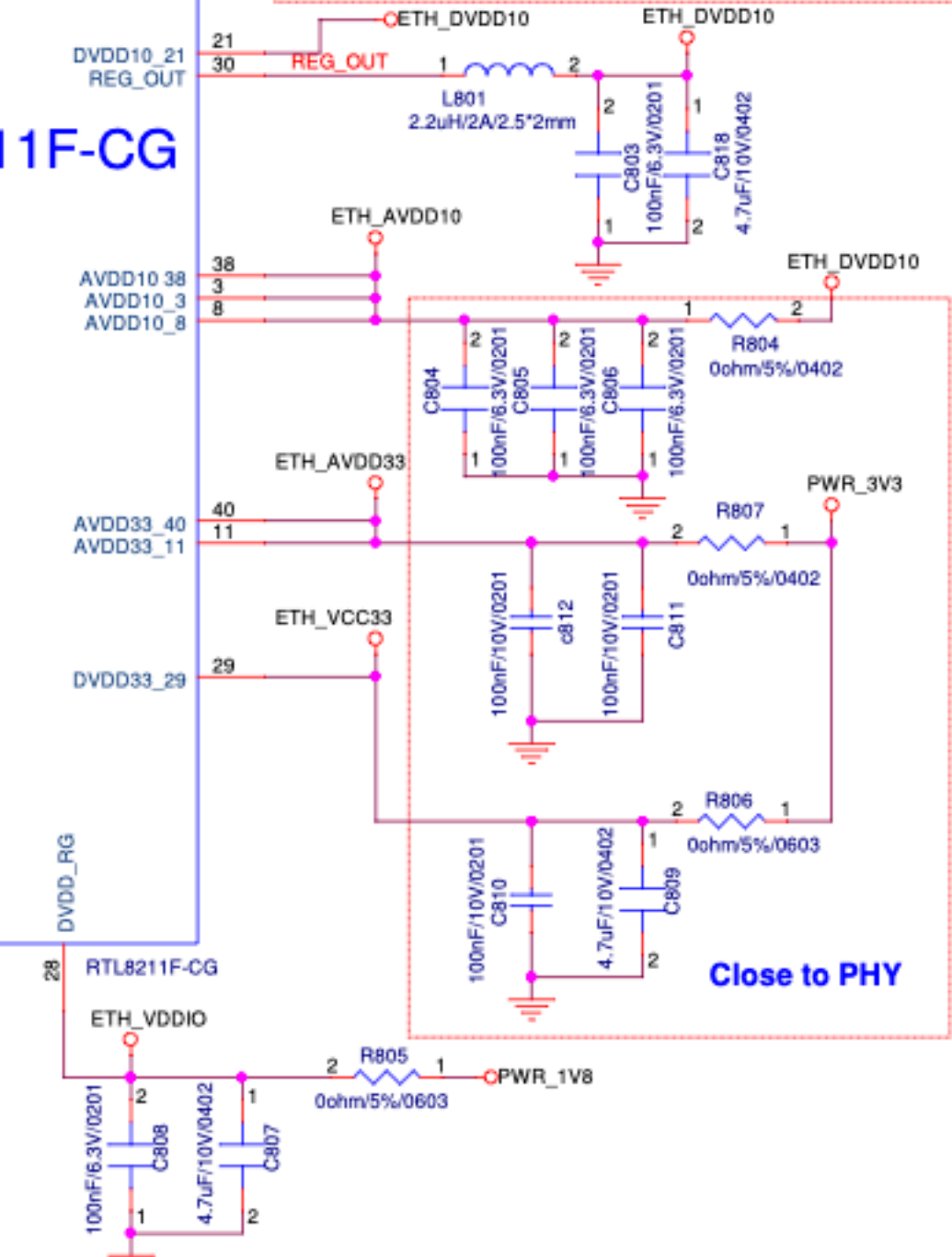
Transformer&RJ45 high-tension line



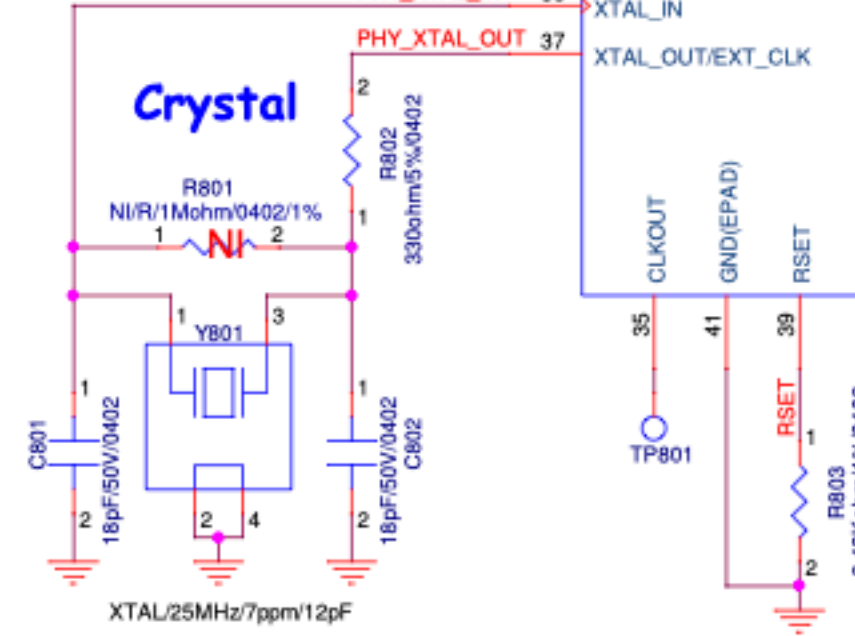
RGMII Voltage Config. Use external P1V8



RTL8211F-CG



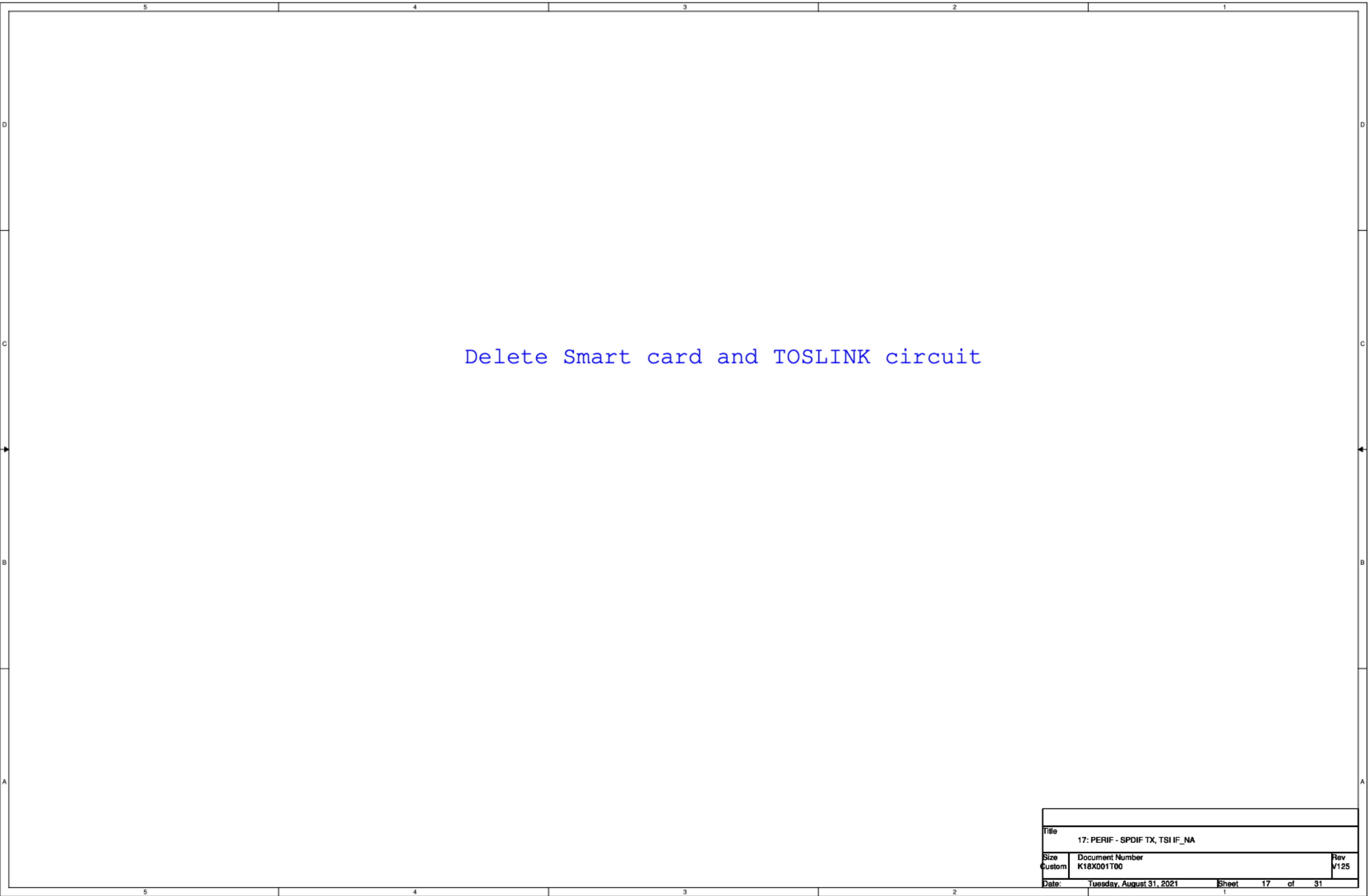
Crystal

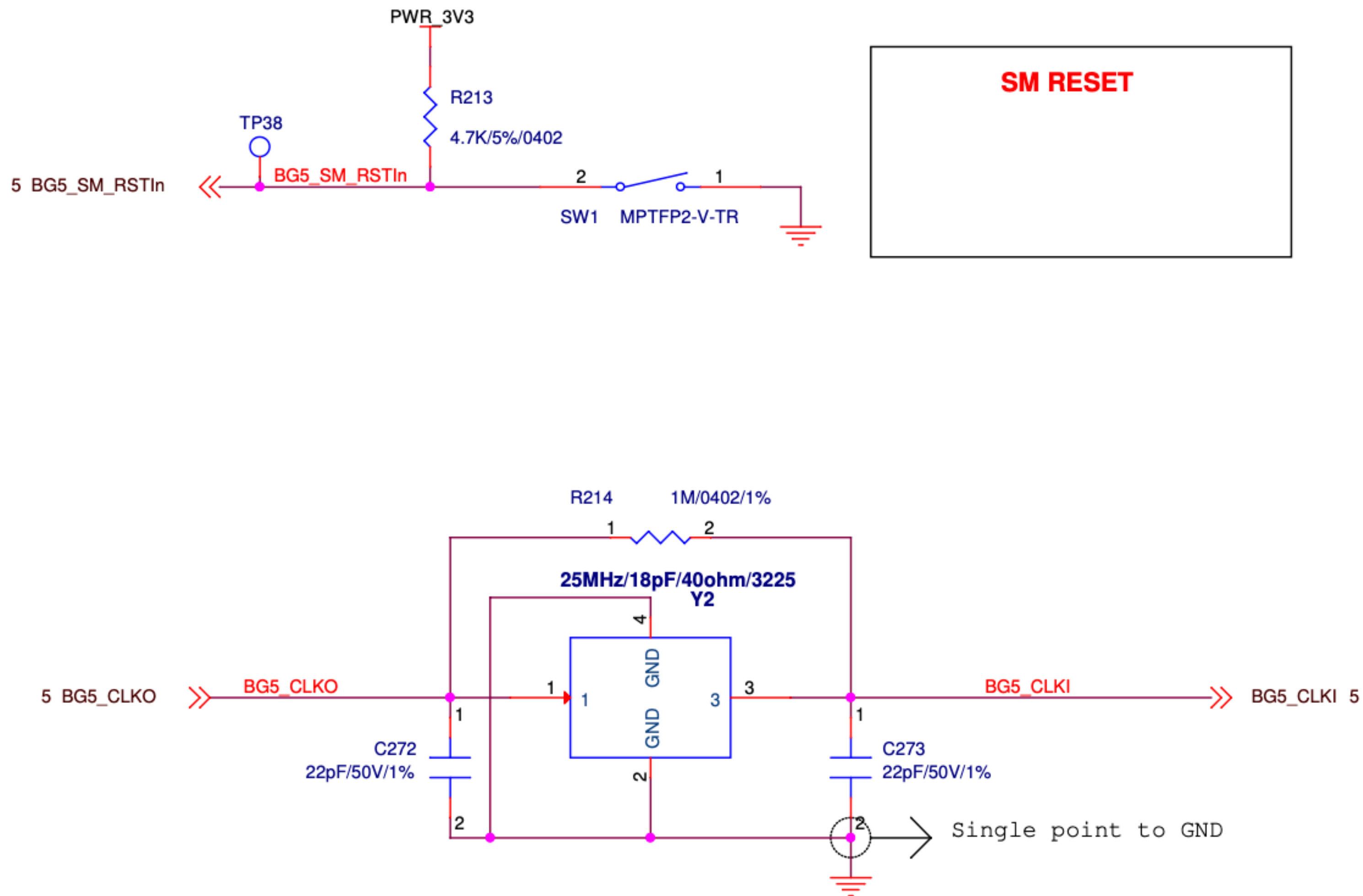


Title			14: PERIF - GbE PHY
Size	Custom	Document Number	K18X001T00
Date:	Tuesday, August 31, 2021	Sheet	14 of 31
		Rev	V125

Delete CX20921-21Z circuit

Title		15: PERIF - Voice Processor_NA	
Size	Document Number		Rev
	K18X001T00		V125
Date:	Tuesday, August 31, 2021	Sheet	15 of 31





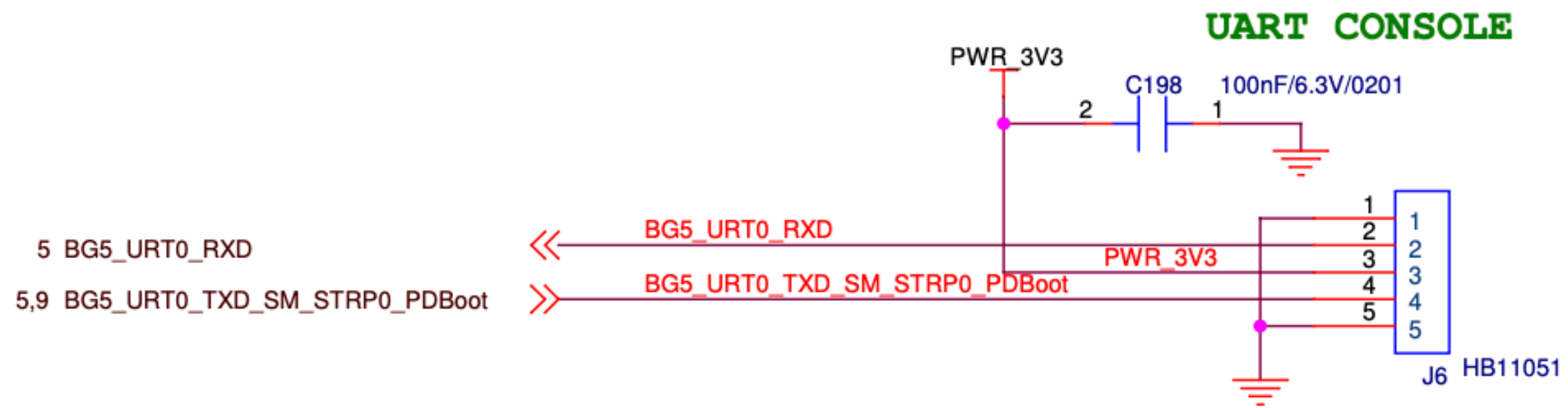
Changes IR receiver to LED board.

Title		
18: PERIF - RST, CLKGEN & IR IN		
Size	Document Number	Rev
	K18X001T00	V125
Date:	Tuesday, August 31, 2021	Sheet 18 of 31

```

Delete J5 JTAG CONN.
Delete J20 CVBS and audio header
Delete FMJ01 BMJ02
for MIC card and Digital audio I2S header

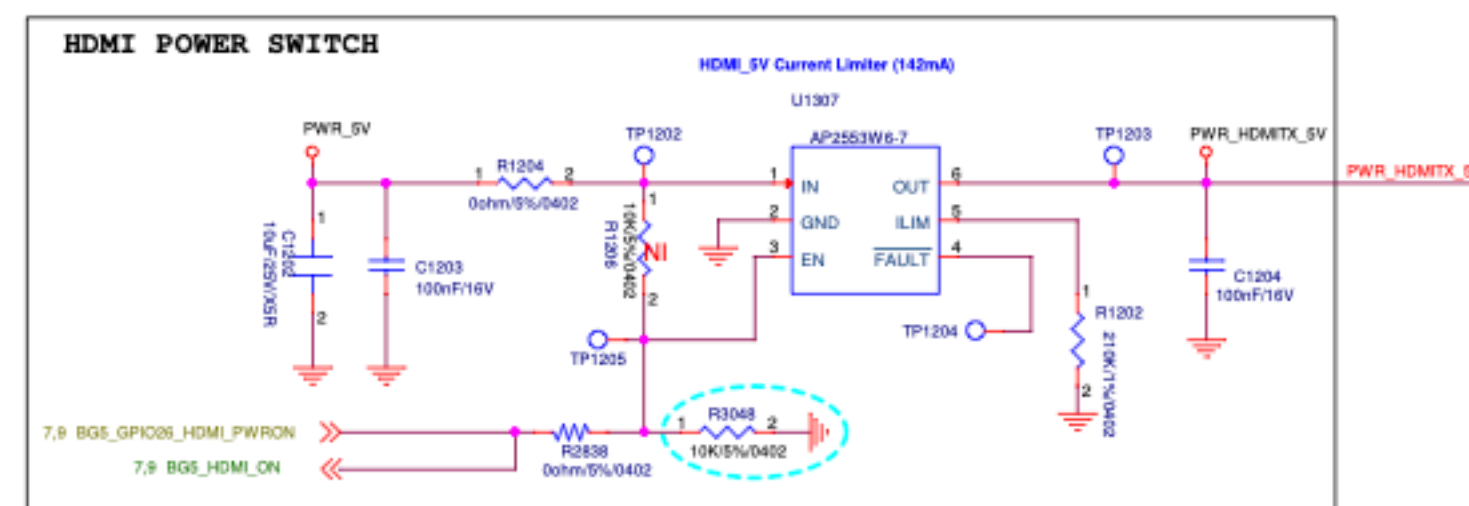
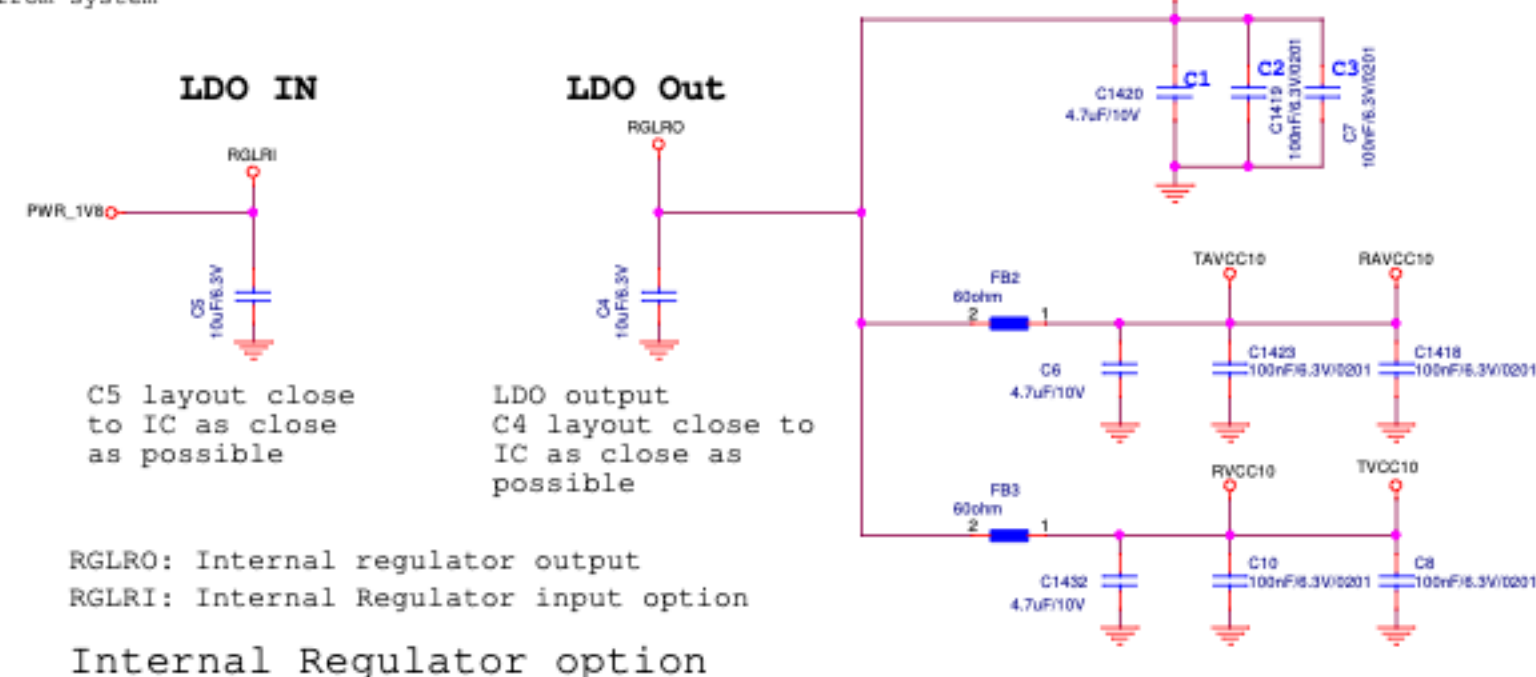
```



Title			
19: CONN - DEBUG			
Size	Document Number	Rev	
A	K18X001T00	V125	
Date:	Tuesday, August 31, 2021	Sheet	19 of 31

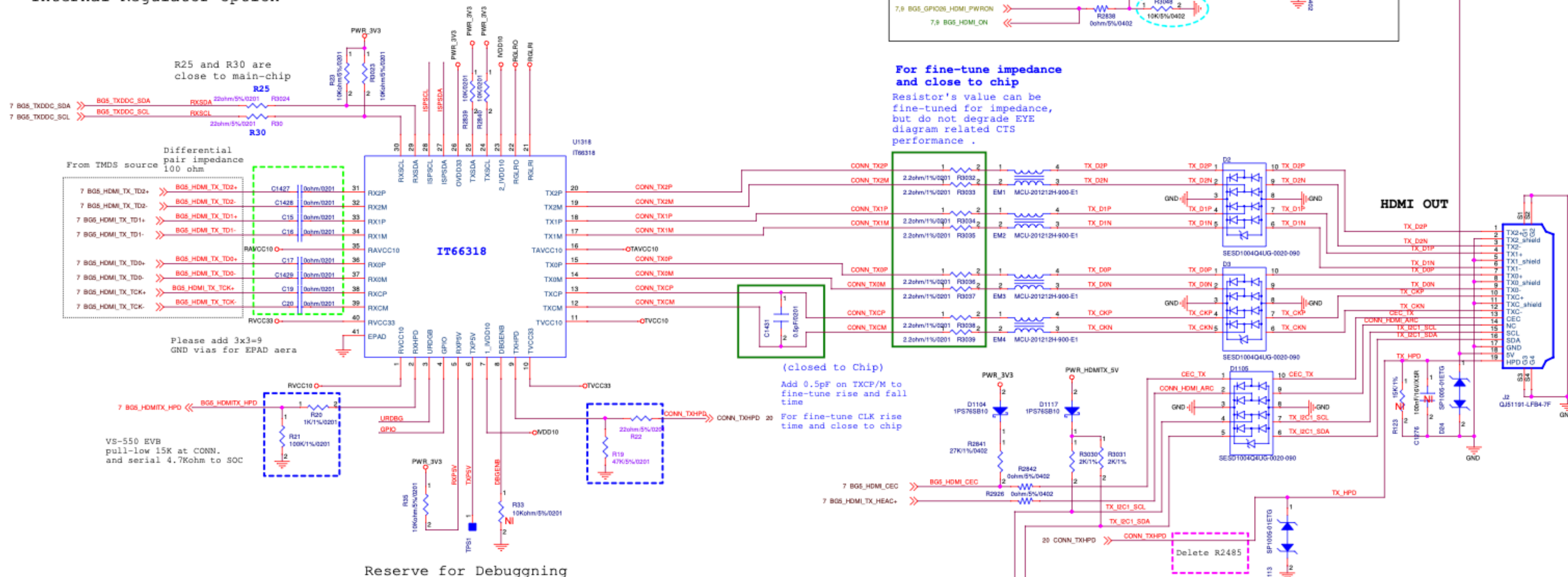
SYS_1V2 is
power 1.2V-1.8V
from system

C1 and C2 layout is close to IC pin 7.
C3 layout is close to IC pin 23.



For fine-tune impedance
and close to chip

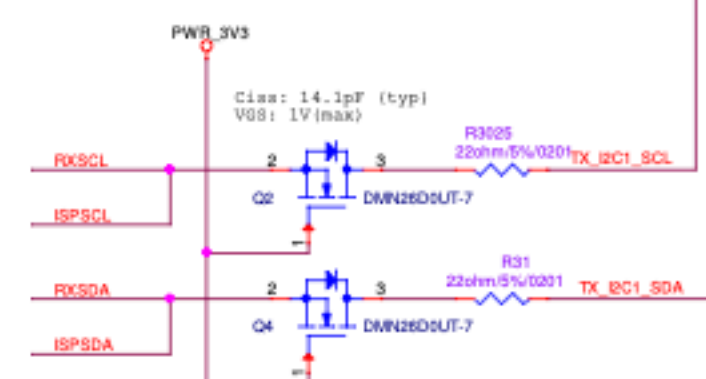
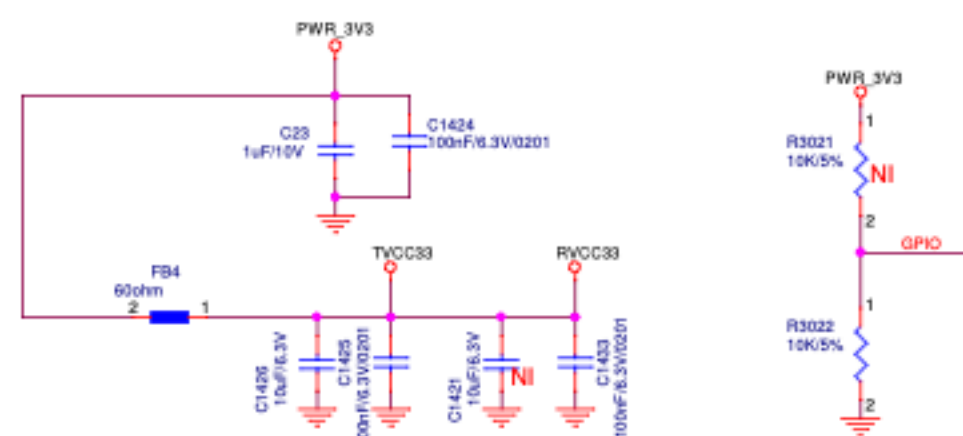
Resistor's value can be fine-tuned for impedance, but do not degrade EYE diagram related CTS performance .



Reserve for Debugging

Reserved Trapping Setting

Output Swing	GPIO	URDBG
Level 1 (Lowest)	0	0
Level 2 (Default)	0	1
Level 3	1	0
Level 4 (Highest)	1	1

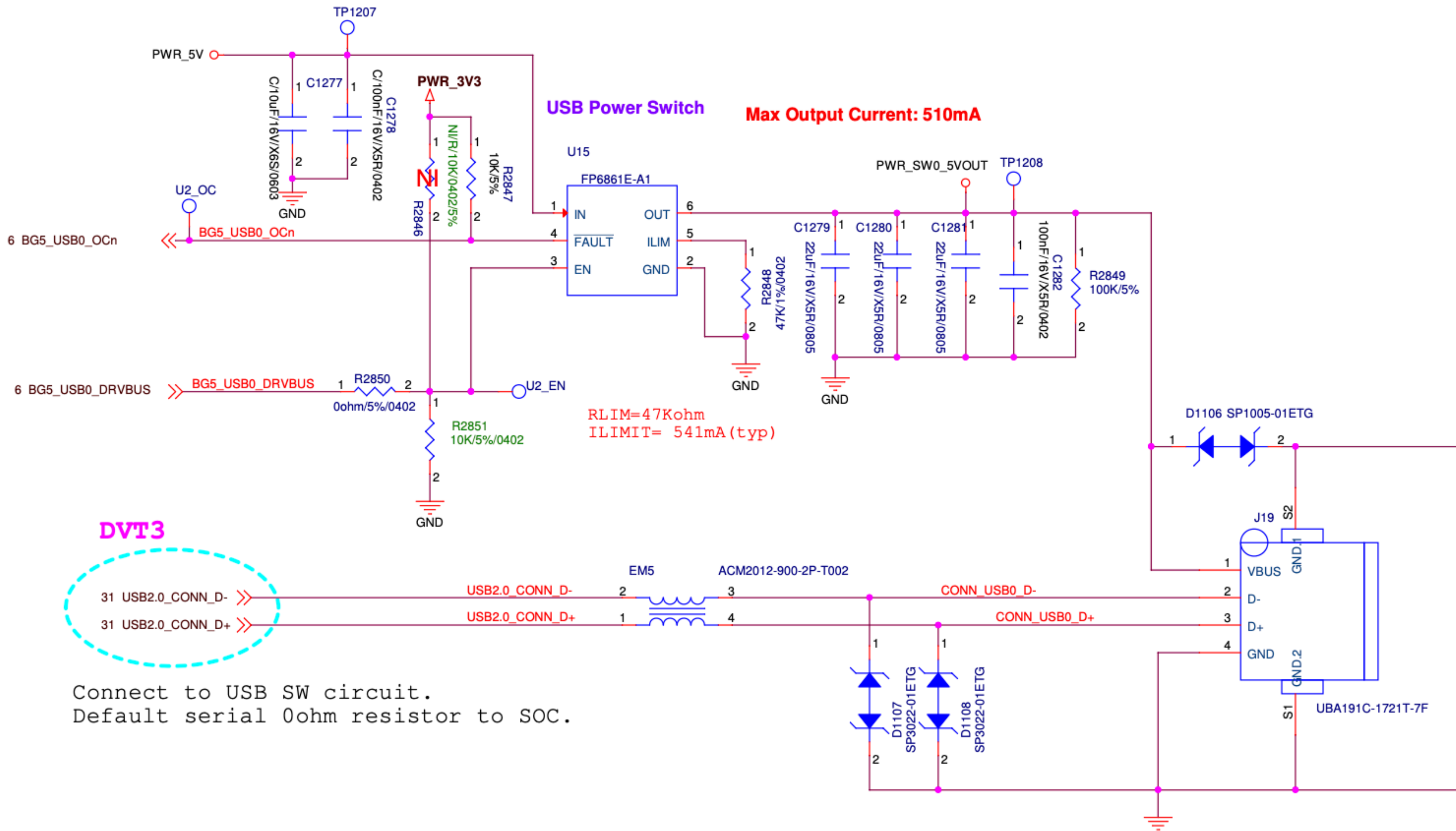


TXDDC LEVEL SHIFTER

5					4					3					2					1				
D																								
C																								
→																								
B																								
A																								
																				</				

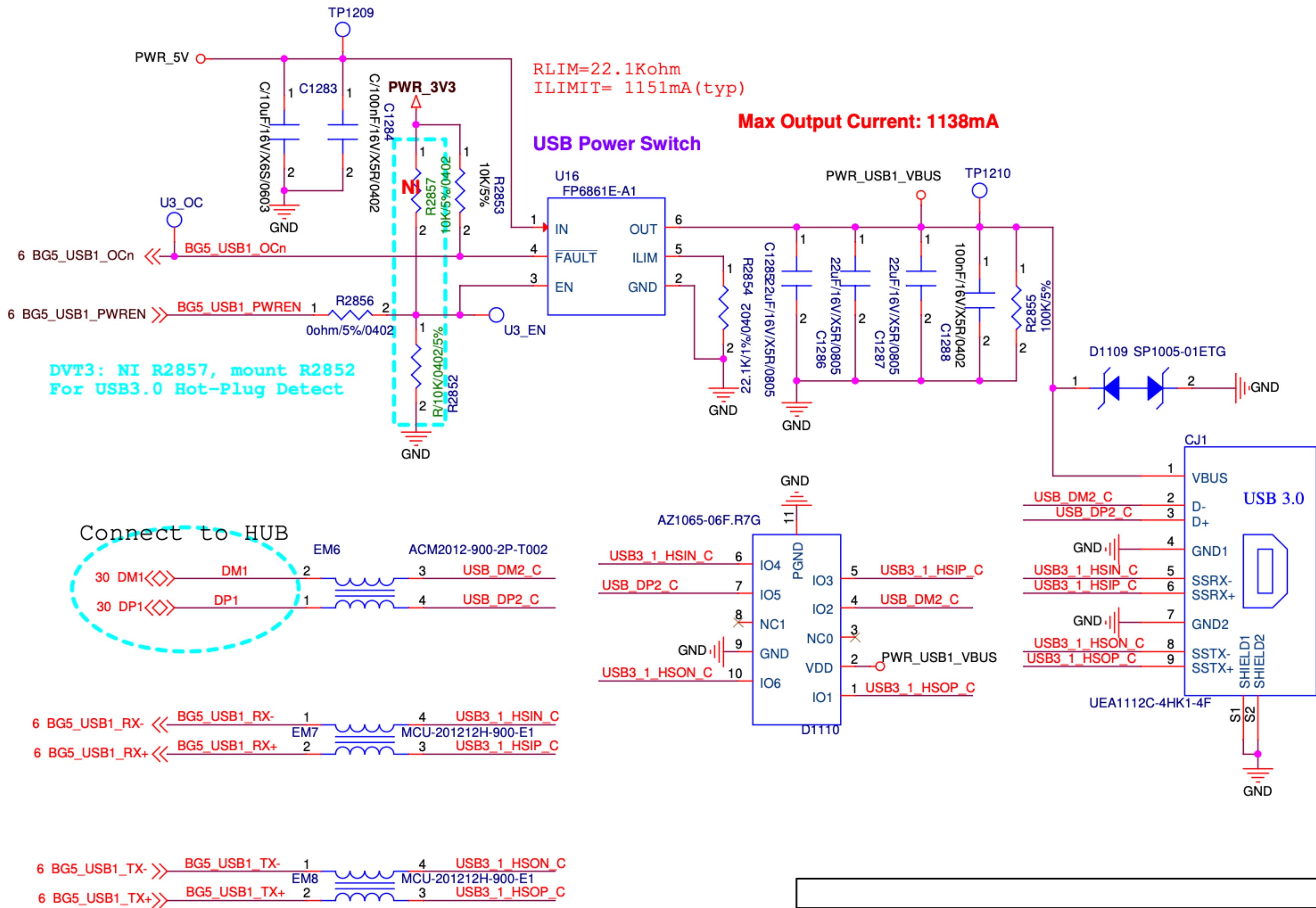
Delete PCIe and J18 (Smart card) card circuit

Title		22: CONN - Mini PCIe_NA	
Size A	Document Number K18X001T00		Rev V125
Date:	Tuesday, August 31, 2021	Sheet	22 of 31

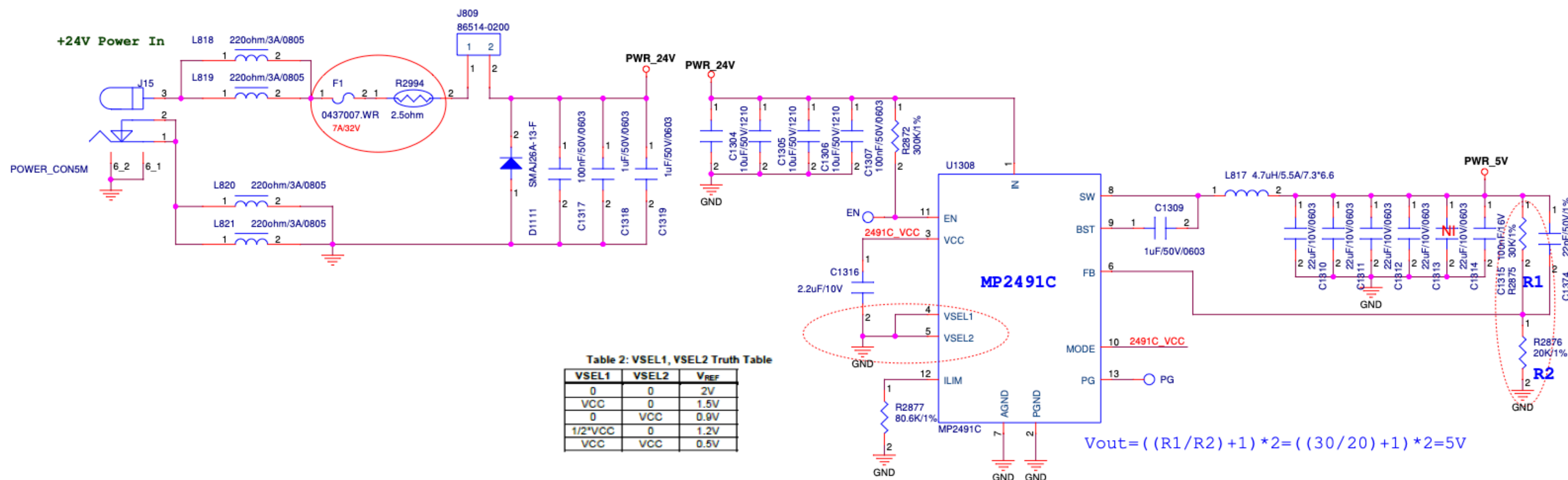


Delete SATA CONN. circuit

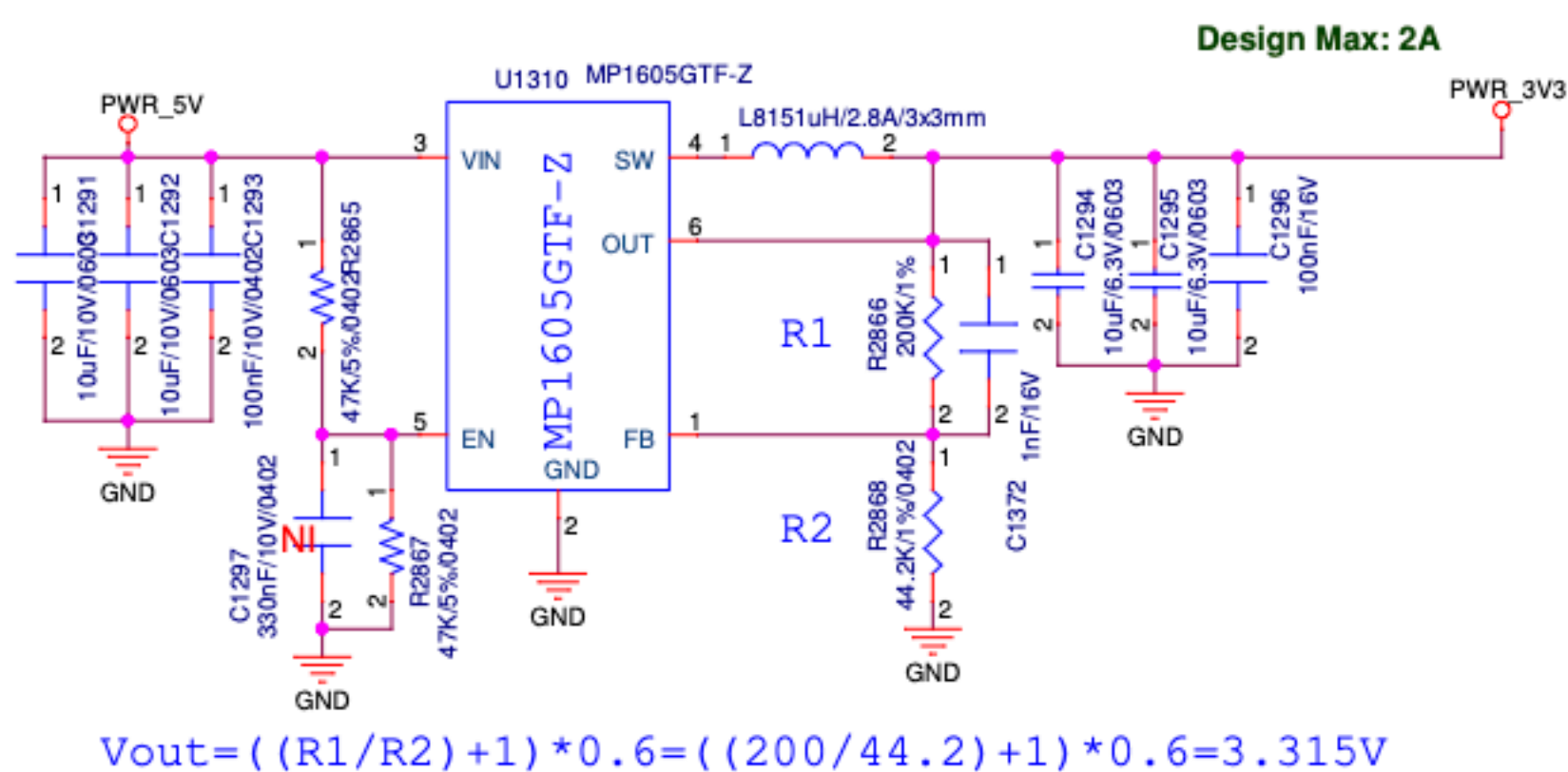
Title		
23: CONN - USB 2.0		
Size	Document Number	Rev
Custom	K18X001T00	V125
Date:	Tuesday, August 31, 2021	Sheet 23 of 31



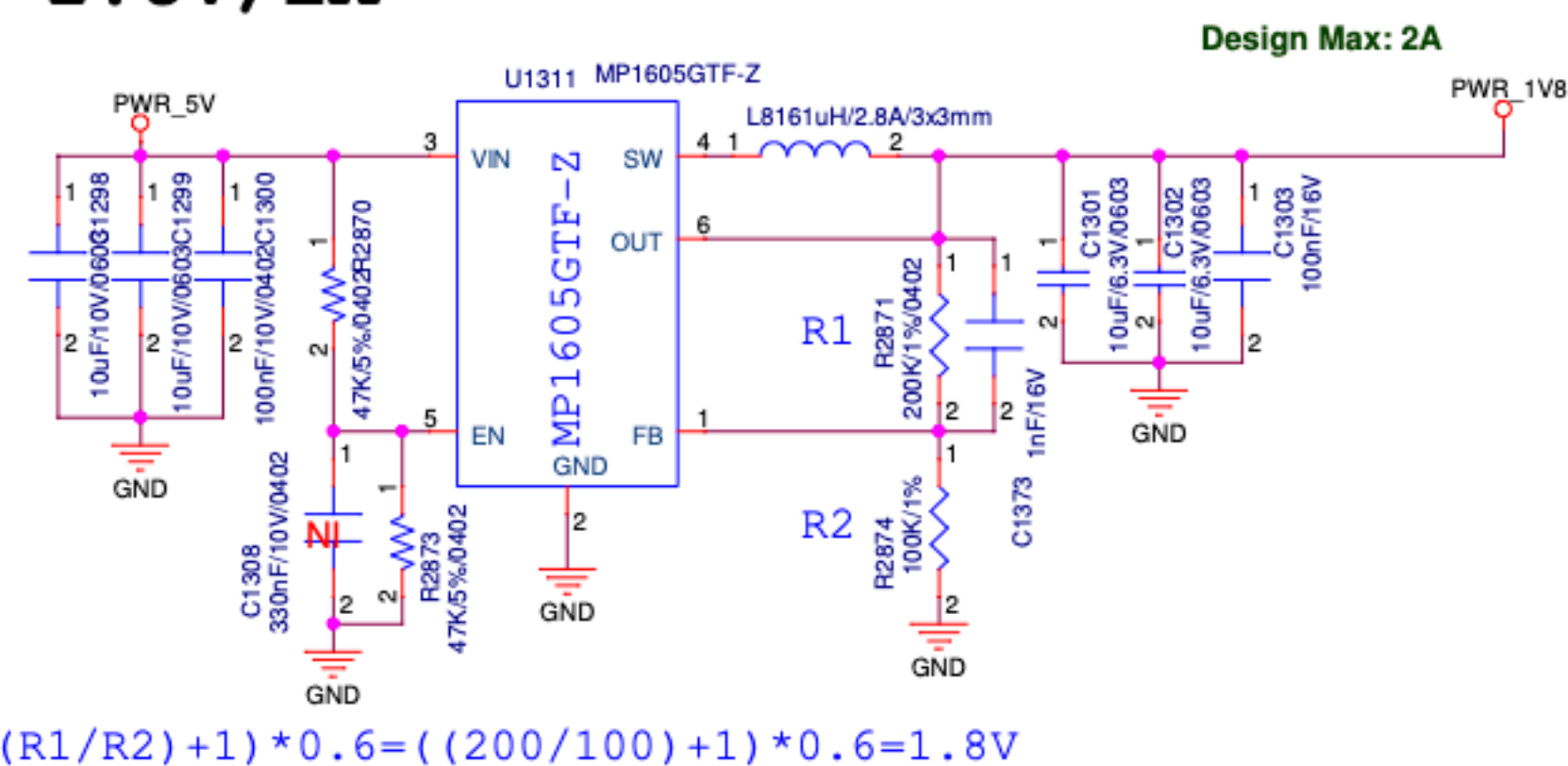
Title		
24: CONN - USB 3.0		
Size	Document Number	Rev
A	K18X001T00	V125
Date:	Tuesday, August 31, 2021	Sheet 24 of 31



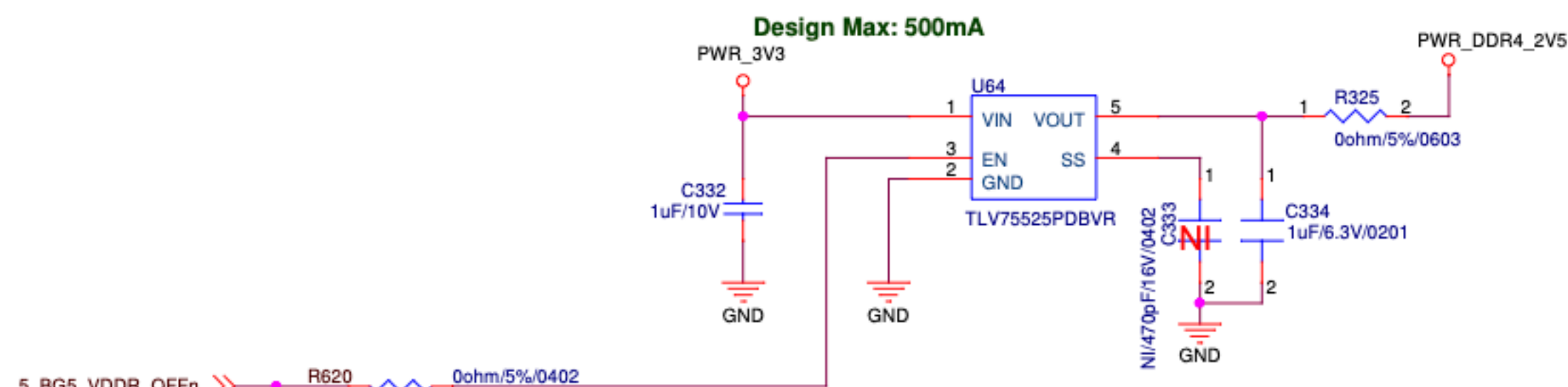
3.3V/2A



1.8V/2A

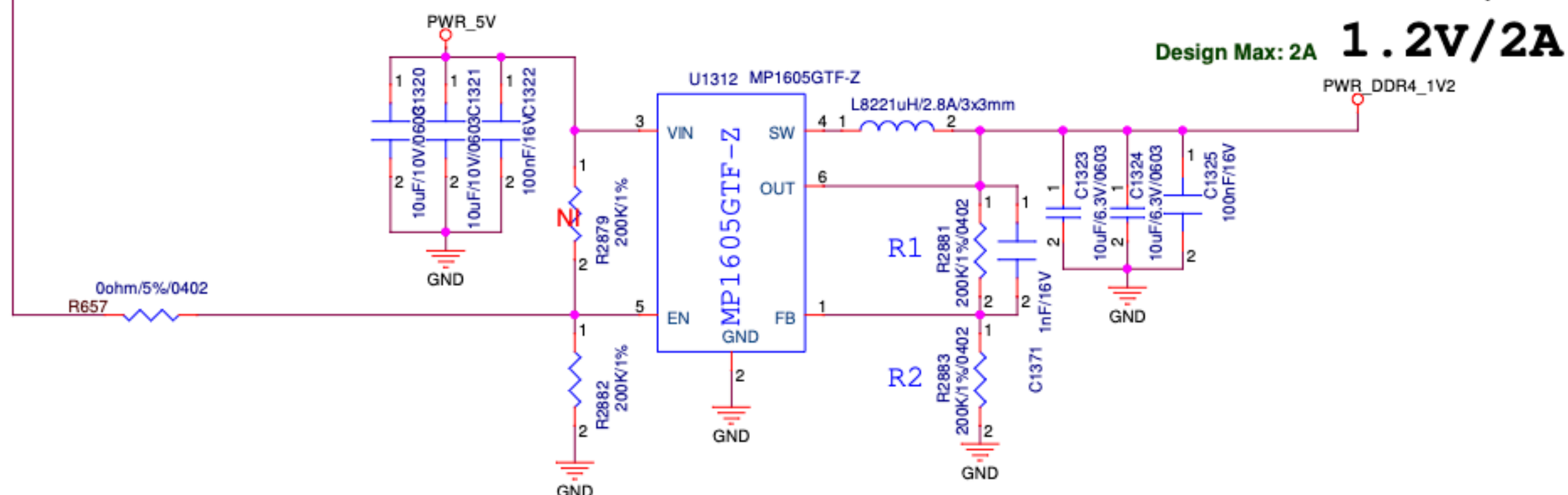


2.5V/0.3A for All DDR4 Devices



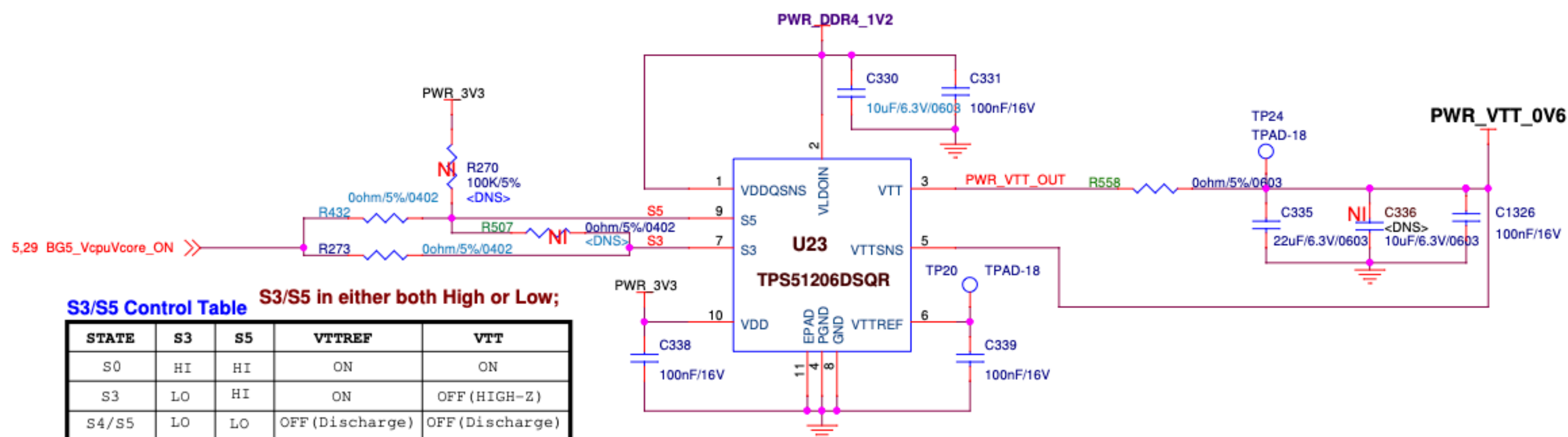
Delete Q20 Q21 circuit,
Because RTL8211 unuse 2V5

1.2V/2A for All DDR4 PHY and Devices x4;



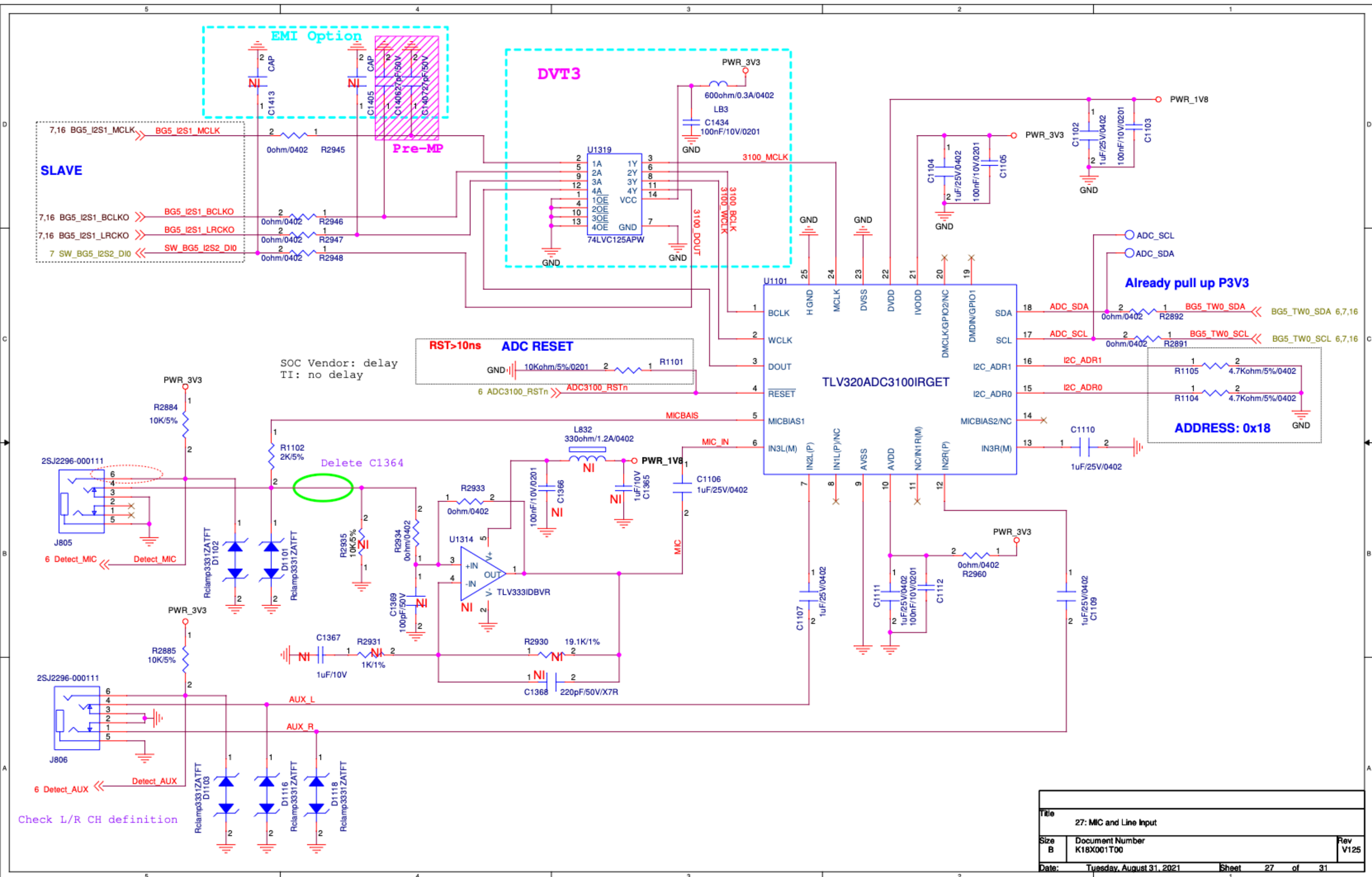
$$V_{out} = ((R1/R2) + 1) * 0.6 = ((200/200) + 1) * 0.6 = 1.2V$$

VTT (0.6V) 1.2A Supply for DDR4 Devices;

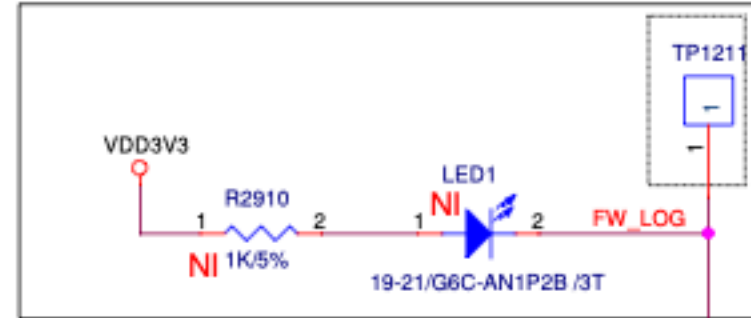


S3/S5 Control Table **S3/S5 in either both High or Low;**

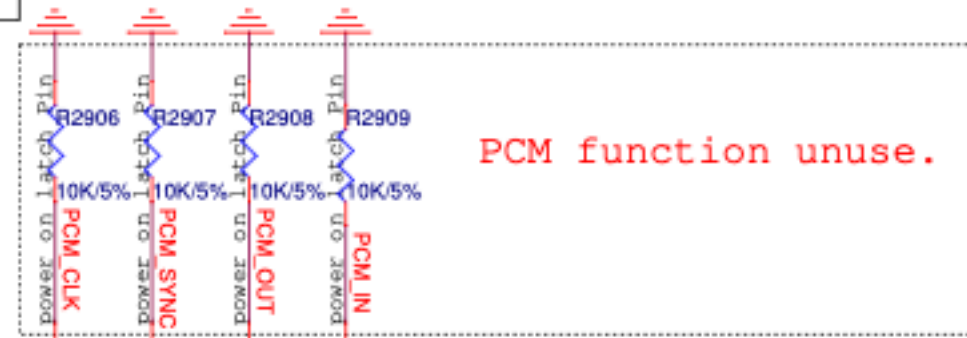
STATE	S3	S5	VTTREF	VTT
S0	HI	HI	ON	ON
S3	LO	HI	ON	OFF (HIGH-Z)
S4/S5	LO	LO	OFF (Discharge)	OFF (Discharge)



Note:
If SPS mode, then R33 10 kohm pull-low, R32 NC and L4 2.2 uH.
If LDO mode, then R33 NC, R32 10 kohm pull-high and L4 0 ohm.



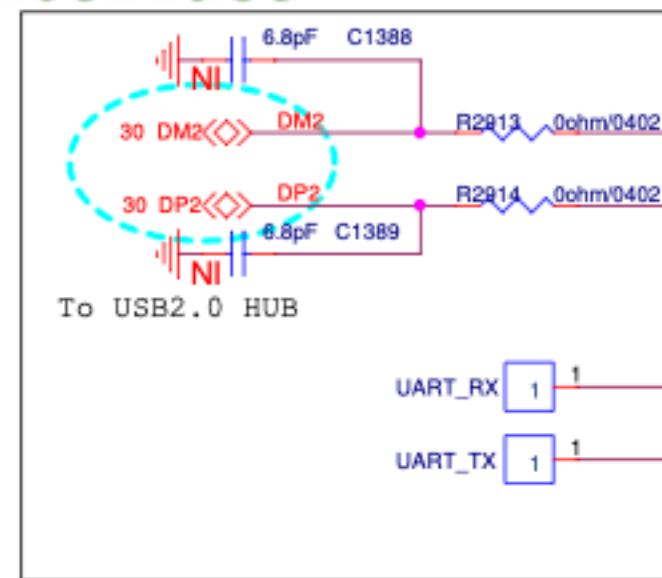
Optional connection to HOST



Note:
WLAN_ACT: Reserved interface for RTK, it could be used as GPIO, add a 10 kohm resistor pull low to GND.

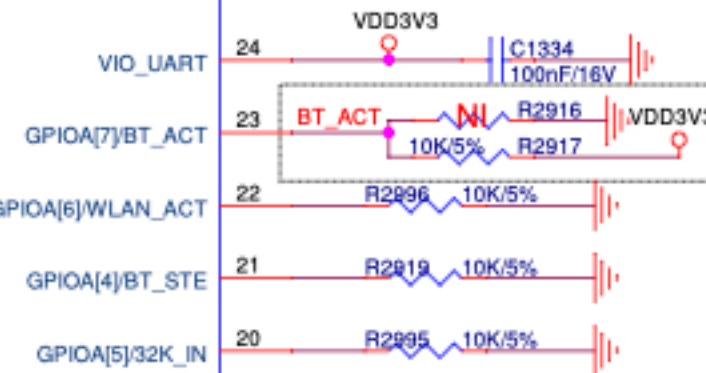
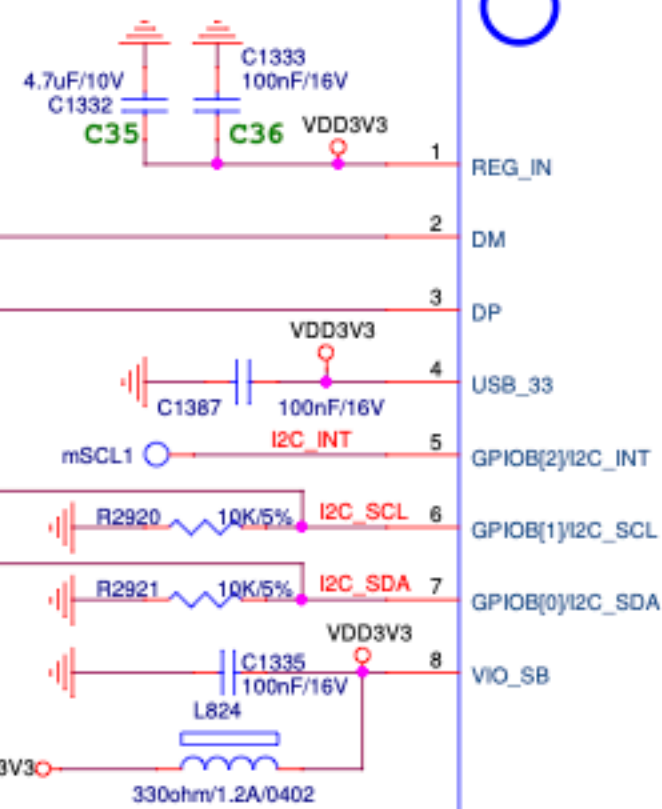
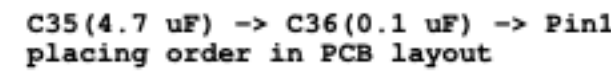
Note:
3.3 V power pin recommended cap type is X5R/10V or above.
1.2 V power pin recommended cap type is X5R/6.3V or above.
RF power pin (Pin 13, 14, 16 & 17) cap value can not
be less than 1 uF.

BQB certification interface

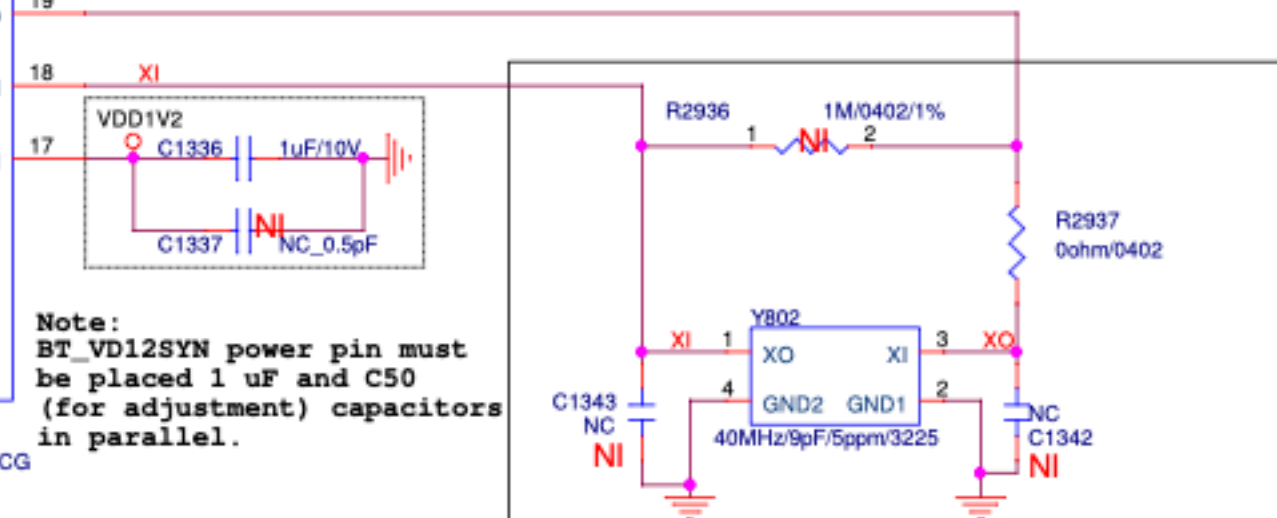


Note:
I2C_SCL & I2C_SDA are BQB Uart
for BQB certification.

Must be placed reserved test points
and could be disconnected with host
module for BQB certification by 0 ohm
resistor.



Note:
BT_ACT is "SPS_LDO_SEL" power on latch pin
Selection of 1.2V Power Supply Mode:
1.If SPS mode is selected, a 10 kohm is placed
connected to GND. L4 should be placed 2.2 uH.
2.If LDO mode is selected, a 10 kohm is placed
connected to VDD3V3. L4 should be placed 0 ohm.



Note:

1. The spec of 40 MHz xtal is with recommended loading cap 9 pF.
2. The loading capacitance is implemented in RTL8761BTV IC, C34 & C36 could be NC but must be placed for reservation.

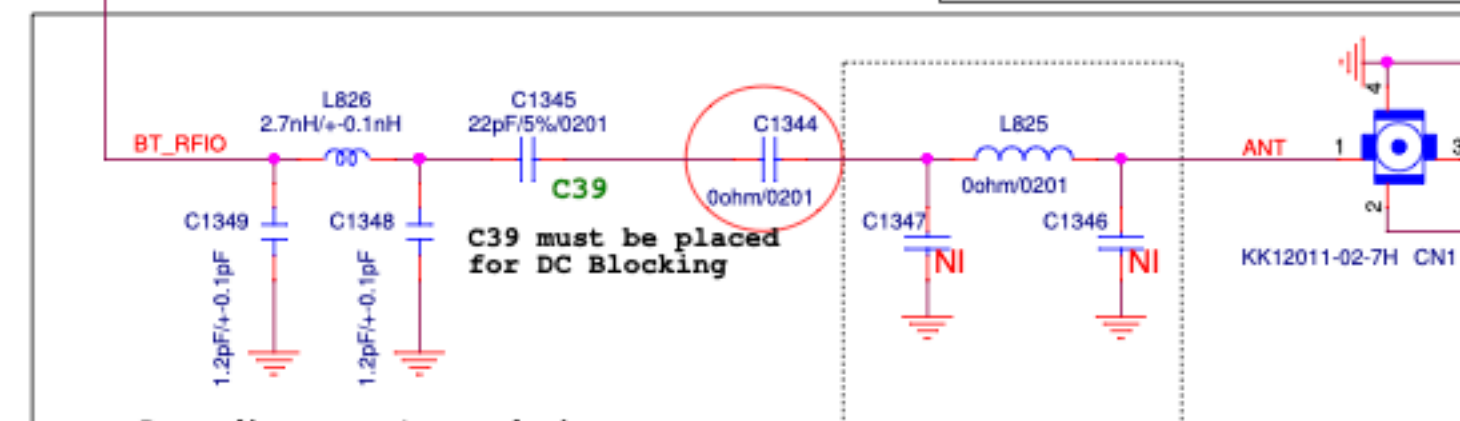
40 MHz xtal clock



	I/O Type	Active	Normal
PIN10 HOST_WAKE_BT	IN		
PIN11 BT_WAKE_HOST	OUT	High	Low
PIN12 DIS_BT_N (Reset)	IN	Low	High

Note:
BT_WAKE_HOST is "EEPROM_SEL"
power on latch pin.
Must be placed the pull-low 10 k Ω
resistor to GND.

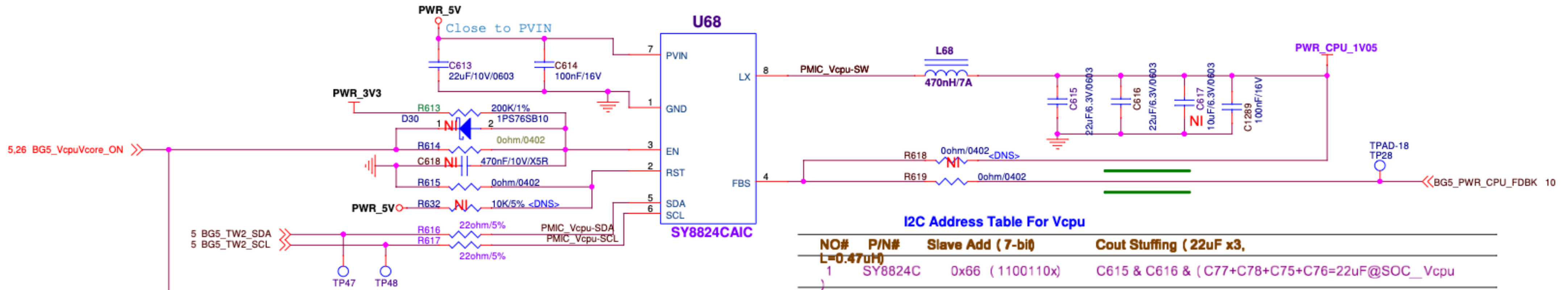
Note:
"DIS_BT_N" pin could be
connected to the host to
implement reset function



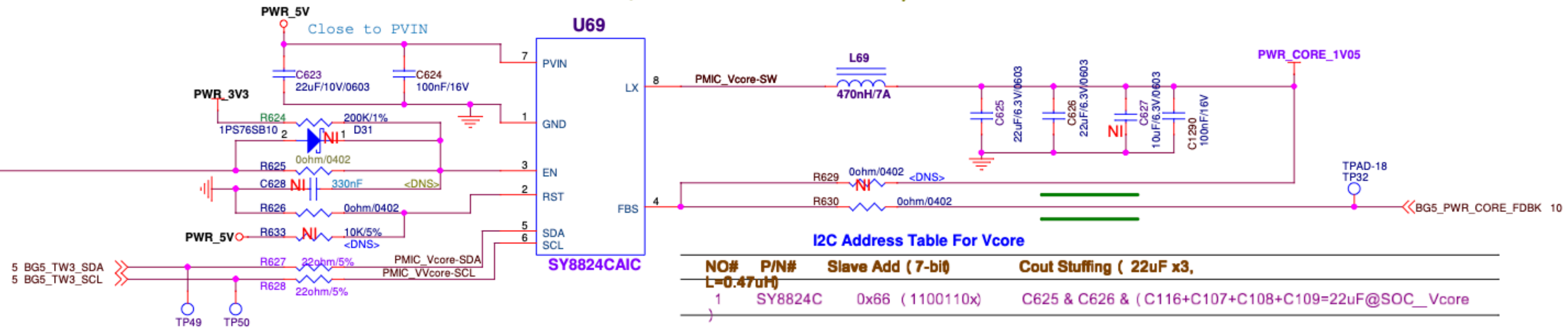
RFIO & pi-matching circuit

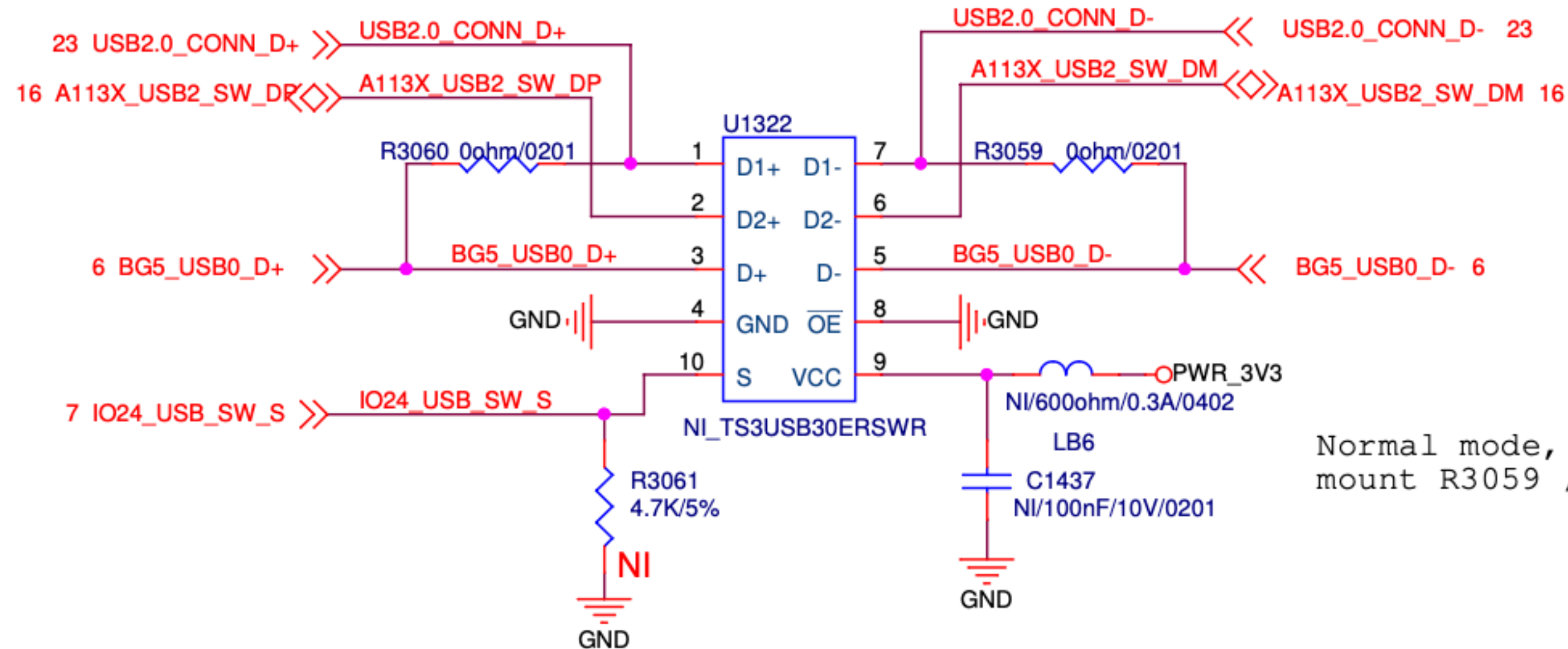
Title			
28: BT RTL8761BTV			
Size	Document Number	Rev	
Custom	K18X001T00	V125	
Date:	Tuesday, August 31, 2021	Sheet	28 of 31

Default 1.05V/4A for Vcpu;



Default 1.05V/4A for Vcore;

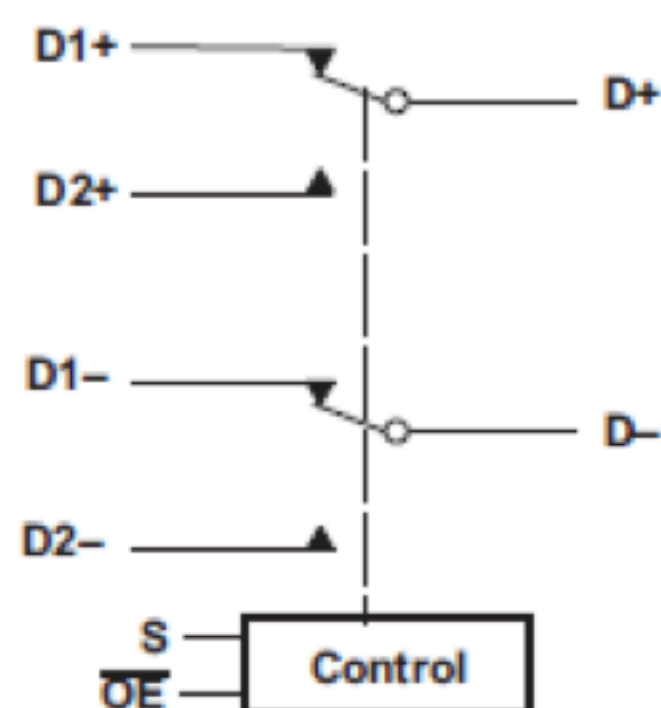




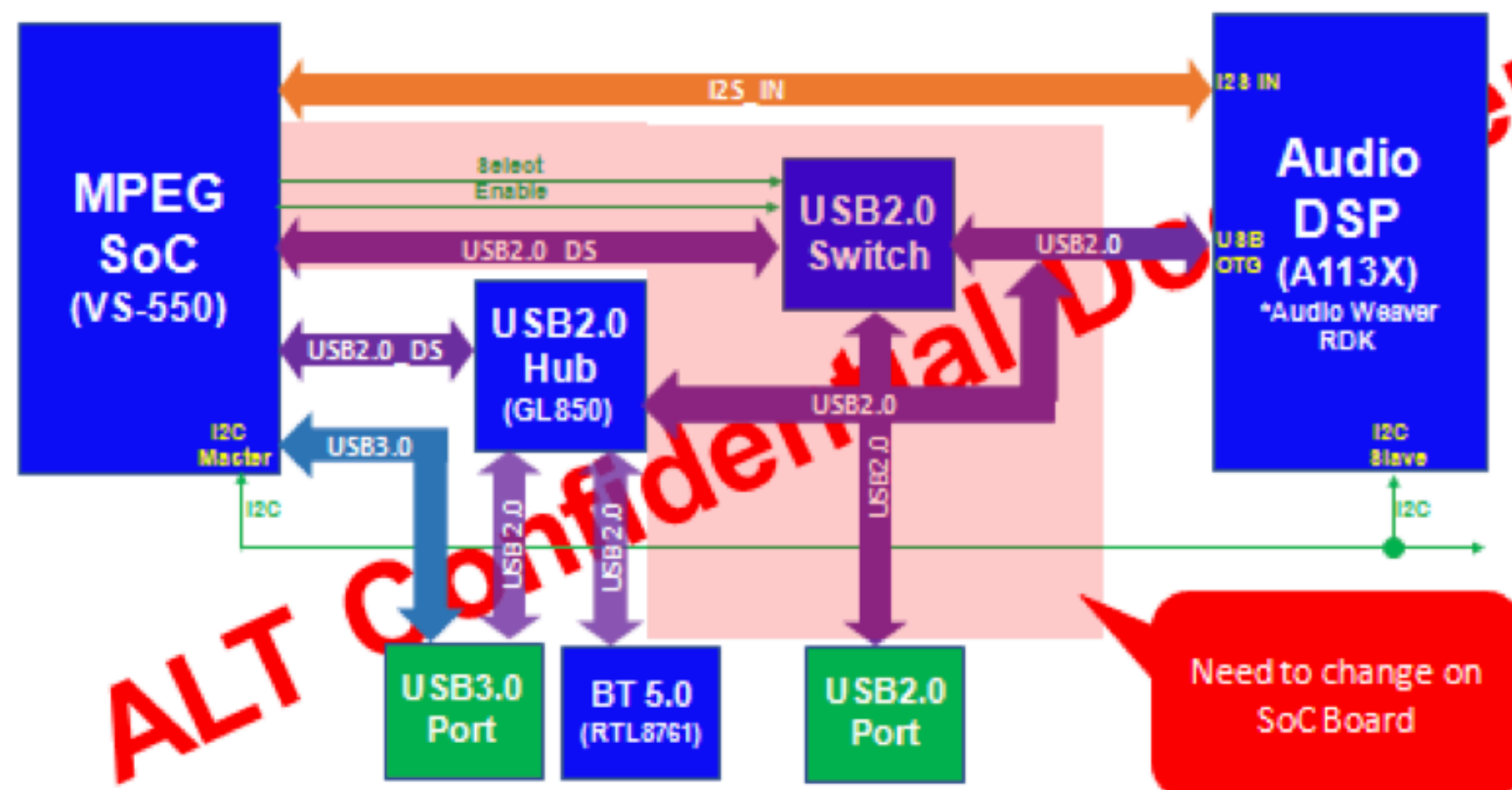
TRUTH TABLE

S	$\overline{\text{OE}}$	FUNCTION
X	H	Disconnect
L	L	D = D1
H	L	D = D2

BLOCK DIAGRAM



● Option3(Reserved option1 & 2)



DVT3 option USB2.0 SW circuit

Title		
31: USB Switch		
Size	Document Number	Rev
A	K18X001T00	V125
Date:	Tuesday, August 31, 2021	Sheet 31 of 31